

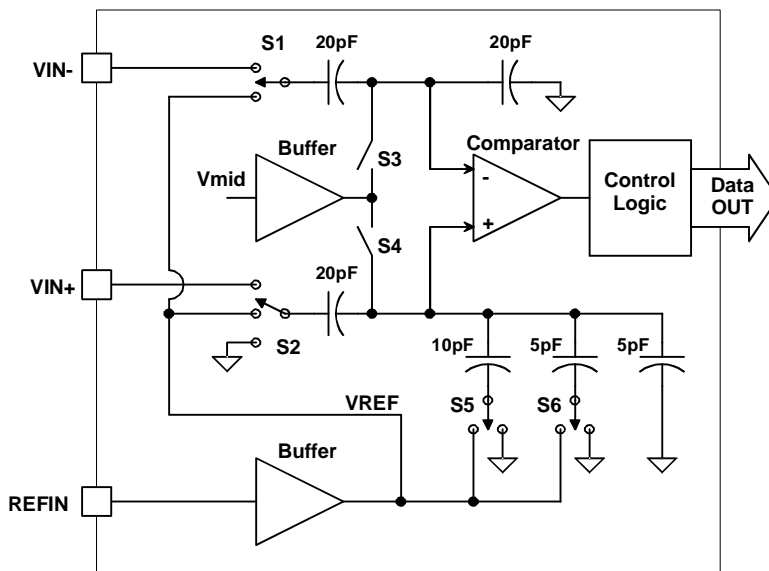
## Designing SAR ADC Drive Circuitry

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### Part I: A Detailed Look at SAR ADC Operation

Designing buffer circuitry for driving successive-approximation (SAR) ADCs requires knowledge of the load that the inputs present. Specifications in data sheets may mislead the user into thinking that analog inputs, for example, are static when in fact they are a very dynamic load. This three-part article will look at the architecture of modern SAR ADCs, and examine the conversion process in detail. In this first part the operation of a modern SAR ADC is discussed. A detailed, step-by-step analysis is then given, illustrating the sampling and conversion process. The final part discusses charge distribution during the sampling process. This analysis will give the user of these devices a better understanding of the inner operations of a charge-redistribution ADC.

### 1. The SAR ADC Structure



**Fig. 1: Representative SAR Input Stage**

Fig. 1 shows a representative three bits of a typical SAR ADC (the ADS8361). Looking at this example, we will examine a three-bit conversion sequence. For our analysis, we will assume that the most significant bit (MSB) capacitor has a value of 20 pF. The capacitor nearest to the MSB capacitor will have half its value, or 10 pF and the least significant bit (LSB) capacitor will have one-quarter of the MSB capacitor value, or 5 pF. A termination capacitor has the same value as the LSB capacitor. The effect of this is that the sum of all the capacitors below the MSB capacitor becomes 20 pF, or the same value as the MSB capacitor.

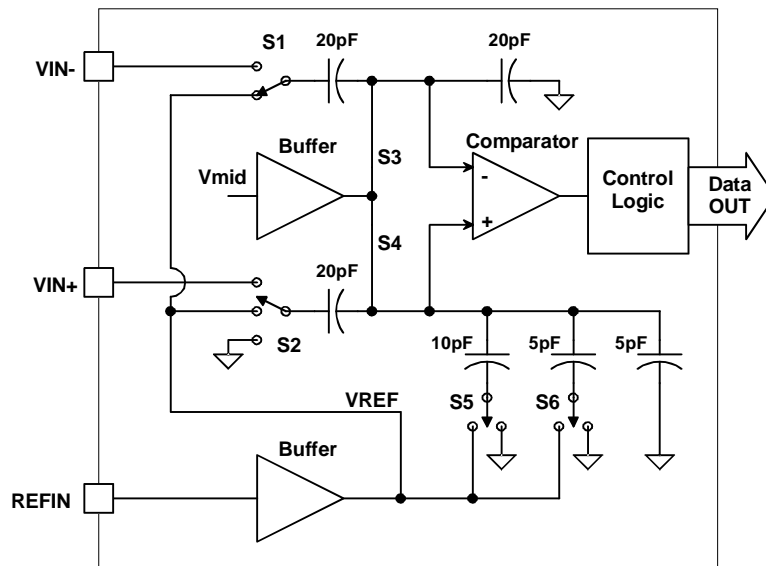
The positive analog input,  $V_{IN+}$ , is sampled by the MSB capacitor through switch S2 and the capacitive conversion network, composed of three capacitors and two switches (S5 and S6). The negative analog input,  $V_{IN-}$ , is sampled by two MSB-valued capacitors in series through switch S1. These two analog inputs, positive and negative, permit this ADC converter to sample differential signals.

The reference voltage is applied to the REFIN input, internally buffered and distributed to all switches that are part of the conversion process. Switches S3 and S4 are connected to the buffered  $V_{mid}$  voltage. The value of  $V_{mid}$  is approximately 2.4 V with a 5-V supply; it will vary in direct proportion with the supply voltage. This buffer is important for proper charge distribution during the sampling period.

The comparator input signals are connected in parallel to switches S3 and S4. During conversion, the comparator output will be processed by the control logic, which will properly set up switches S2, S5 and S6. (Note that this type of architecture is for the ADS8361 and similar, bipolar input range parts. Other parts may have a similar structure, but are not identical.)

## 2. The Sampling Process in Detail

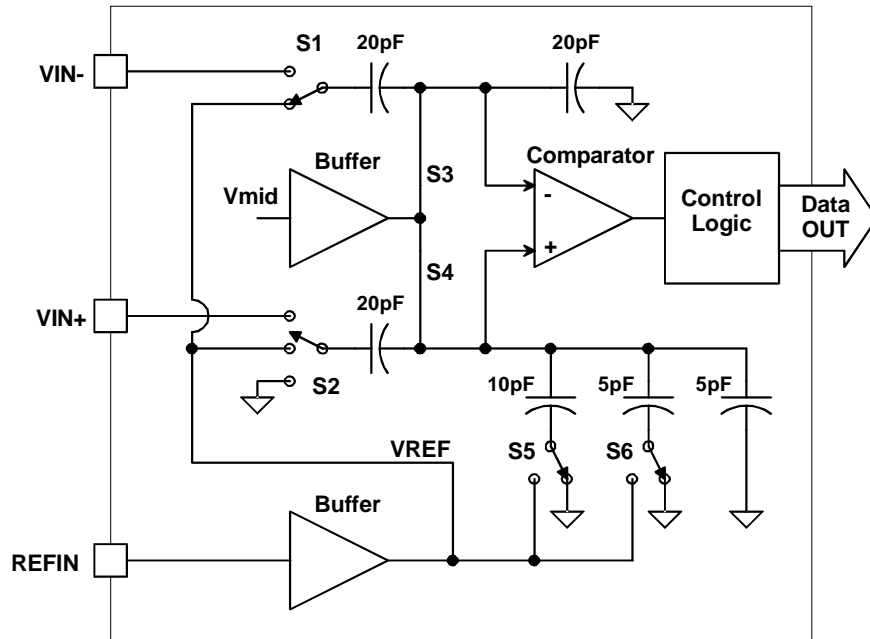
At the end of the conversion process, the ADS8361 automatically goes into the sampling process. The positions of switches S5 and S6 in the capacitive conversion network are unknown, as well as the position of switch S2. Switch S2 can be closed to either ground or the reference voltage. The status of the switches depends on the results of the previous conversion.



**Fig. 2: Beginning of the Sampling Period**

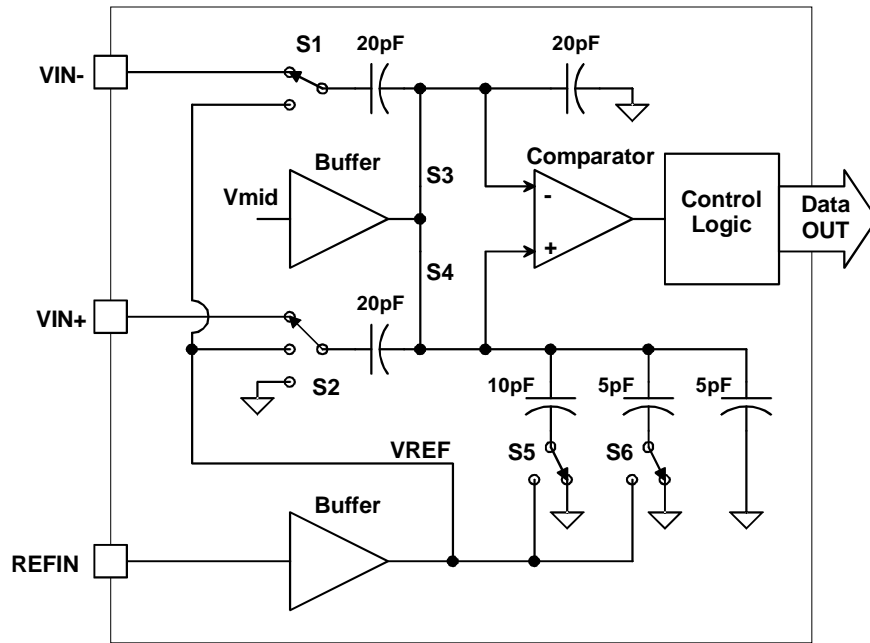
We know that switch S1 is connected to the reference voltage,  $V_{REF}$ . The sampling process initiates closing switches S3 and S4. This short-circuits the comparator inputs and connects them to  $V_{MID}$ . This initial phase of the sampling cycle is shown in Fig. 2.

Because the positions of switches S5 and S6 are unknown, the equivalent capacitance of the network is also unknown. For proper sampling, however, the capacitive conversion network must have an equivalent capacitance that is equal to the MSB capacitor value. To obtain this capacitance, switches S5 and S6 in this step must connect the associated capacitors to the ground terminal. In this way, the positive input, as well as the negative input, of the comparator will be connected over the MSB capacitor equivalent value to ground. This configuration is shown in Fig. 3.



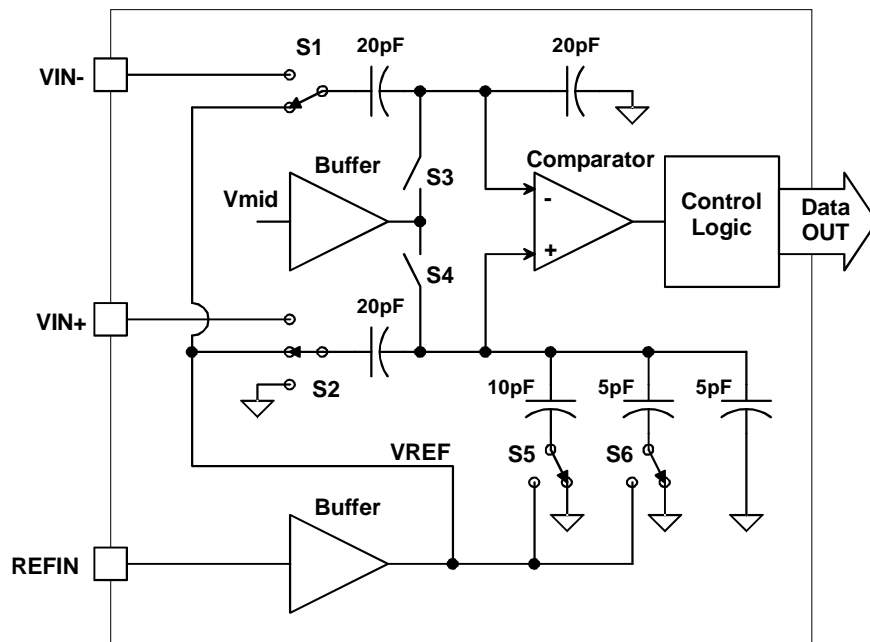
**Fig. 3: Resetting the Value of the Capacitive Conversion Network**

Up to this point, all changes (such as charge distribution and switch positions) only affect the internal operation. The analog input signals were not affected by these changes. In the next step, input switches S1 and S2 close, and the input signal is sampled on the input MSB capacitors. This period is the most critical period and to have accurate results from the conversion, the input buffer must be capable of charging the sampling MSB capacitors to the proper value. The sampling of the input signal is shown in Fig. 4.



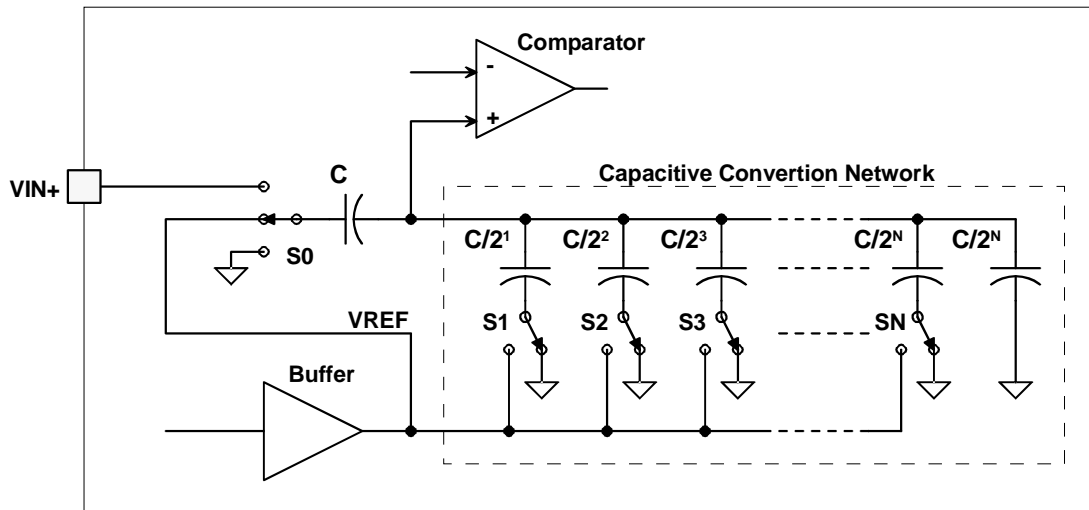
**Fig. 4: Sampling of the Input Signal**

After charging the sampling capacitor with the input voltage, preparation for the conversion cycle starts with opening switches S3 and S4 when the charge on the sampling capacitors will be frozen. Disconnecting the MSB capacitors from the analog inputs VIN+ and VIN- indicates the end of the sampling period. The next step connects the MSB capacitors with switches S1 and S2 to the reference voltage, VREF. Fig. 5 shows the end of the sampling period and the start of the conversion cycle.



**Fig. 5: Start of the Conversion Cycle.**

This representative analysis is for a 3-bit ADC, or a capacitive conversion network that is composed of three capacitors and two switches. This capacitive conversion network can be replaced with the real one (for N-bits SAR ADC) shown in Fig. 6.



**Fig. 6: Capacitive Conversion Network for N-Bits SAR ADC**

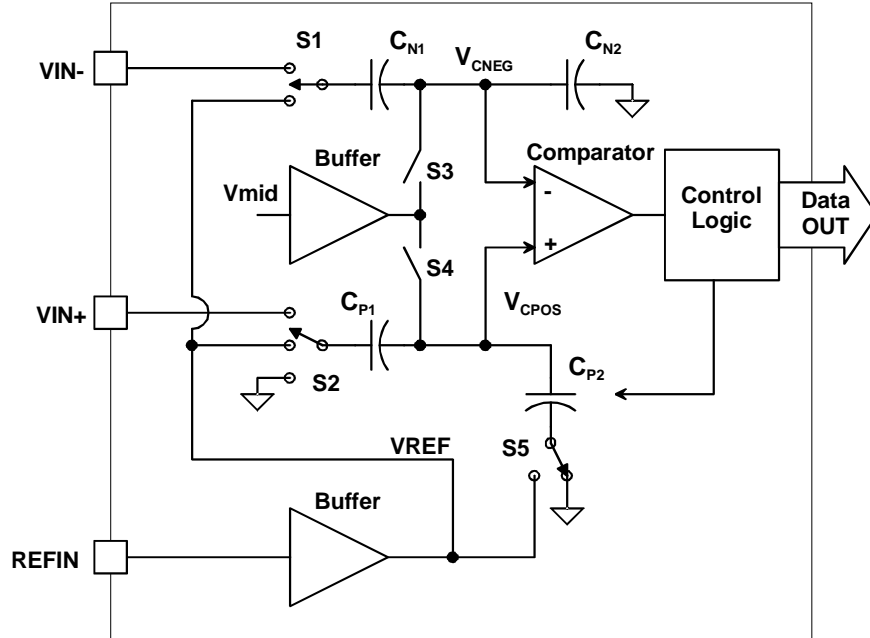
The sampling (or MSB) capacitor connected to switch S0 has the standard value,  $C$ . The capacitive conversion network, as presented in Fig. 6, has an equivalent capacitive value equal to the value of the MSB capacitor. For the N-Bit SAR ADC, the capacitive conversion network will be composed of  $N+1$  capacitors and  $N$  switches.

The first capacitor has a value that is one-half of the standard MSB capacitor value, or  $(0.5 \cdot C)$ . The second capacitor has a value that is one-fourth the value of  $C$ , the third one has a value that is one-eighth the value of  $C$ , and so on. The last two capacitors each have a value that is  $(1/2^N)$  of the value of  $C$ . For a 12-bit SAR ADC,  $N$  is 12; for a 14-Bit SAR ADC,  $N$  is 14, and so on.

The resolution of the SAR ADC is equivalent to the number of switches and capacitors that are in the capacitive conversion network, and their respective values.

### 3. Charge Distribution During the Sampling Process

To explain the matter of charge distribution during the sampling and conversion period, Fig. 7 presents a simplified circuit, equivalent to that of Fig. 1.



**Fig. 7: Simplified SAR ADC Circuit**

The sampling or MSB capacitor (CP1), connected to switch S2 and the positive input, has the standard value  $C$ . The sampling capacitor (CN1) that is connected to switch S1 and the negative input also has the standard value  $C$ . The capacitive conversion network as presented in Fig. 6 has an equivalent capacitive value equal to the value of the MSB capacitor, and is presented as capacitor (CP2) in Fig. 7. The comparator negative input has voltage  $V_{CNEG}$  and the positive input  $V_{CPOS}$ .

The measured signal is connected to the positive input  $V_{IN+}$  and negative input  $V_{IN-}$ . As described in section 2, the sampling of the input signal starts by closing switches S3 and S4. In this way, the positive input voltage,  $V_{CPOS}$ , to the comparator is equal to the middle voltage,  $V_{MID}$ . At the same time, the negative input voltage  $V_{CNEG}$  to the comparator is also equal to the middle voltage,  $V_{MID}$ . The next step is to close switch S5 to  $V_{GND}$ . Switches S1 and S2 remain open. Now the ADC is ready to sample the input signal. The sampling process starts by closing input switches S1 and S2 to the input analog signal.

After a transition period of approximately 500 ns (depending on the applied input buffer circuit), the voltages stabilize and the new situation is present. The existing configuration from Fig. 7 demonstrates the positive charge, QPS, that charges capacitors CP1 and CP2. Equation 1 explains this charge distribution sequence.

$$Q_{PS} = (V_{MID} - V_{IN+}) \times C_{P1} + (V_{MID} - V_{GND}) \times C_{P2} \quad \text{Eq. 1}$$

Following the same procedure, the negative charge QNS that charges capacitors CN1 and CN2 is described by Equation 2:

$$Q_{NS} = (V_{MID} - V_{IN-}) \times C_{N1} + (V_{MID} - V_{GND}) \times C_{N2} \quad \text{Eq. 2}$$

The next step in the sampling process starts when switches S3 and S4 open. In this way, the negative VCNEG and positive VCPOS input voltages into the comparator are not tied together anymore. The charge QPS on the capacitors CP1 and CP2 as well the charge QNS on the capacitors CN1 and CN2 will be frozen. The input switches S1 and S2 open next. To start the comparing or the conversion process, switches S1 and S2 close to the VREF position. Now the charge of the two capacitors CP1 and CP2 is distributed as explained by Equation 3:

$$Q_{PC1} = (V_{CPOS} - V_{REF}) \times C_{P1} + (V_{CPOS} - V_{GND}) \times C_{P2} \quad \text{Eq. 3}$$

Following the same process, the charge of capacitors CN1 and CN2 is described by Equation (4):

$$Q_{NC1} = (V_{CNEG} - V_{REF}) \times C_{N1} + (V_{CNEG} - V_{GND}) \times C_{N2} \quad \text{Eq. 4}$$

The charge of capacitors CP1 and CP2 during the sampling and conversion processes is the same. Combining Equation 1 and Equation 3 and substituting the voltage VGND with 0, the result is Equation 5:

$$V_{CPOS} = V_{MID} + \frac{C_{P1}}{C_{P1} + C_{P2}} \times (V_{REF} - V_{IN+}) \quad \text{Eq. 5}$$

A similar calculation is applied to the negative side of the input stage. If the charge of capacitors CN1 and CN2 during the sampling and conversion process is the same, combining Equation 2 and Equation 4 and substituting the voltage VGND with 0 produces Equation 6:

$$V_{CNEG} = V_{MID} + \frac{C_{N1}}{C_{N1} + C_{N2}} \times (V_{REF} - V_{IN-}) \quad \text{Eq. 6}$$

Equations 5 and 6 present the positive input voltage VCPOS and negative input voltage VCNEG into the comparator as a function of the positive input voltage VIN+ and negative input voltage VIN-. Capacitors CN1 and CN2 are equal and have the same value. The negative input comparator voltage VCNEG (referring to Equation 6) is constant during the entire conversion period, and can be described by Equation 7:

$$V_{CNEG} = V_{MID} + \frac{V_{REF} - V_{IN-}}{2} \quad \text{Eq. 7}$$

The conversion process is accomplished by comparing the dynamic signal VCPOS (described by Equation 5) with a constant voltage VCNEG (described by Equation 7). Fig. 7 shows that capacitor CP2 is an equivalent presentation. During the conversion process, capacitor CP2 will change its value from the maximum value equal to MSB capacitor, CP1, to the lower value so that the difference between voltages VCPOS and VCNEG is minimized.

#### 4. Conversion

The sampling of the input signal ends and conversion begins when switches S3 and S4 are opened, capturing the input analog signal. Next, the sample switches S1 and S2 are opened, as explained in Section 3. The descriptions in this section refer to Fig. 7:.

##### The Negative Input Signal

First, we look at the negative input signal side. The comparator negative input node at S3 is VCNEG. The negative input signal side is set up as an input-signal-voltage-dependent reference for the comparator. Switch S1 switches from VIN- to VREF. The charge stored in the negative input signal side capacitors CN1 and CN2, during conversion QNC1, is equivalent to the charge stored during sampling QNS. The charge sum on capacitors CN1 and CN2 is conserved. Thus, the VCNEG is described by Equation 7 and remains constant during conversion.

In the case of single-ended signals, VIN- is connected and equal to VREF, so as a consequence very little charge redistribution occurs on the negative input signal side after sampling. When a differential signal is sampled, the VIN- will differ from VREF; then the charge redistributes, presenting a load on the reference buffer circuit.

##### The Positive Input Signal

On the positive input signal side, the transition from sampling into testing the MSB is similar to the negative input signal side. We will refer to the comparator positive input node at S4 as VPOS. The positive input signal side is set up as a variable input signal voltage for the comparator. The switch S2 switches from VIN+ to VREF and switch S5 remains connected to ground. The charge stored in the positive input signal side capacitors CP1 and CP2, during conversion QPC1, is equivalent to the charge stored during sampling QPS. The charge on the total capacitor array is the same during conversion as during sampling. The charge sum on capacitors CP1 and CP2 is conserved. Thus, the VPOS is described by Equation 5 and is variable during conversion.

As in the first instance, switch S2 is connected to VREF, switch S5 to ground, and capacitors CP1 and CP2 have the same value, so Equation 5 can be rewritten as Equation 8:

$$V_{CPOS} = V_{MID} + \frac{V_{REF} - V_{IN+}}{2} \quad \text{Eq. 8}$$

### Testing the Bits

At the end of the first clock cycle, voltages VCPOS and VCNEG are compared by the comparator, resolving the value of the MSB to either a 1 or a 0. This value will be latched into the SAR control logic. If the value is 1, the CP1 capacitor remains connected over switch S2 to VREF. If the value is 0, it will be connected over the same switch to ground.

To understand the rest of the conversion process, we need to refer to the capacitive conversion network presented in Fig. 6. At the same clock edge, the control logic of the SAR converter shifts to test the next most significant bit, which is referred to as bit 2. Switch S1 from Fig. 6 switches from ground to VREF. The charge on the capacitor array will again be redistributed, placing a load on the reference buffer.

The state of the capacitor array is now a function of the decision made during the MSB test. Each bit test that follows will be a function of the preceding bit test. The voltage on VCPOS becomes dependent on which capacitors from the capacitive conversion network are connected to VREF and which are connected to ground. Under these conditions, the positive input voltage to comparator can be described by Equation 9:

$$V_{CPOS} = \frac{2 \cdot V_{MID} \cdot C - V_{IN+} \cdot C + V_{REF} \cdot \sum C_{REF}}{2 \cdot C} \quad \text{Eq. 9}$$

where  $\sum C_{REF}$  represents the sum of the capacitors tied to the reference voltage.

Now, assume that the first bit tested high. The MSB capacitor is held at the reference voltage, and the second bit is tied to the reference for testing. Referring to Fig. 6 and replacing C with 20 pF, there will now be 30 pF of capacitance tied to the reference voltage. The voltage across this capacitance is given by Equation 10:

$$V_{CPOS} = \frac{2 \cdot V_{MID} \cdot 20 \text{ pF} - V_{IN+} \cdot 20 \text{ pF} + V_{REF} \cdot 30 \text{ pF}}{2 \cdot 20 \text{ pF}} \quad \text{Eq. 10}$$

The 30 pF occurs because the MSB sampling capacitor C (with the value of 20 pF) is tied to VREF as a result of the first decision, and the next capacitor connected to switch S1 with the value of (0.5\*C), or 10 pF, is also tied to VREF for testing.

### The End of Conversion

This sequence continues until the final bit is tested. We can assume that at the end of the conversion, the negative input signal into the comparator, VCNEG, is equal to the positive input signal into the comparator, VCPOS. Combining Equation 7 and Equation 9, we can relate VCPOS and VCPOS by Equation 11. The purpose of the conversion is to drive the positive input signal into the comparator VCPOS to an approximately equivalent value of VCNEG:

$$V_{MID} - \frac{1}{2} \cdot V_{IN+} + V_{REF} \cdot \frac{\sum C_{REF}}{2 \cdot C} = V_{MID} - \frac{1}{2} \cdot V_{IN-} + \frac{1}{2} \cdot V_{REF} \quad \text{Eq. 11}$$

It is insightful to note that for any given resolution, with any given input signal, the state of the capacitors at the end of conversion is given by Equation 12, which is obtained by solving Equation 11 for the input signal, or (VIN+ – VIN–):

$$V_{IN+} - V_{IN-} = V_{REF} \cdot \left( \frac{\sum C_{REF}}{C} - 1 \right) \quad \text{Eq. 12}$$

The more positive the value of the input signal (or VIN+ – VIN–), the greater the proportion of capacitors tied to the reference voltage. At positive full-scale, +VREF, all capacitors from the capacitor conversion network will be tied to VREF. Alternately, if VIN+–VIN– is equal to -VREF, then no capacitors are tied to VREF, or all of them are tied to ground.

Since the ratio of the sum of the capacitors, or  $\Sigma C_{REF}/C$ , is in the range of 0 to 2, then from Equation 12 we can see that the input analog signal VIN+–VIN– is in the range of –VREF up to +VREF.

Note that the ADS8361 complements the most significant bit in the output code. The MSB indicates negative signals with a 1. If the MSB is a 1 internally, indicating the input signal is positive, it will be a 0 in the output code.

## Conclusion

In this article, a better understanding of the internal operation of a modern SAR ADC is gained by looking at the sampling and conversion process in detail. The load that a SAR ADC presents to its driver circuitry was also examined and design criteria developed in order to optimize solutions for this difficult design problem.

## About The Authors

Rick Downs is applications engineering manager for Texas Instruments' Data Acquisition Products group in Tucson, AZ. Over the past 20 years, he has held various positions in applications and marketing of analog semiconductors, with focuses on audio, data acquisition, digital temperature sensors and battery management products. Rick holds a bachelor of science in Electrical Engineering from the University of Arizona, and has three patents. He has authored several articles and application notes on analog topics, and prepared and delivered several seminars on data acquisition.

Miroslav Oljacac has over 17 years of design and manager experience in the field of motor control and power conversion. His design experience ranges from the several watt to megawatt range. Miroslav currently specify and support products that provides motor control solutions targeted at high precision motor control applications. He earned his BSEE and MSEE degrees in electrical engineering from the Electrotechnical University in Belgrade (Yugoslavia) in 1986 and 1988.

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