

Designing SAR ADC Drive Circuitry

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Part III: Designing The Optimal Input Drive Circuit For SAR ADCs

Parts I and II of this series [2, 3] discussed the basic operation of a SAR-type ADC, and why a SAR converter requires drive circuitry of a particular topology. In this last installment, we introduce a procedure for designing this drive circuitry. In doing so, we focus on the op amp requirements and some of the techniques for optimizing the op amp and ADC system. Sometimes, a slight change to the ADC timing can make all the difference in an application. Furthermore, there are some optimizations that can be made to the RC circuit in front of the SAR. However, these adjustments are very application-specific and need careful consideration.

Limitation Of Op Amp Output Stage

Rail-to-rail operation of an op amp can refer to its input stage, its output stage, or both. As a buffer for driving the input of a SAR ADC, we are more concerned about the rail-to-rail output capability of the op amp. This output drive capability generally specifies how close the output can swing to the power-supply rails. This specification is provided in most product data sheets for low-frequency or dc output signals. A better understanding of the output swing capability can help us to determine the optimum working point for given conditions when driving the ADC input.

To determine the limits of the output stage, a rail-to-rail op amp, with a rail voltage of 5 V, the input signal was offset by 2.5 V: half the power-supply voltage. The amplifier (a TI OPA365) was configured in a voltage follower (or gain of +1) configuration. The peak-to-peak input ac signal was increased in amplitude from 0 V to 5 V, up to the power-supply voltage level. Measuring total harmonic distortion plus noise (THD+N) on the output of the op amp for different peak-to-peak output voltages gives us an idea of when the output stage arrives at its limitation. Fig. 1 illustrates the measured signal.

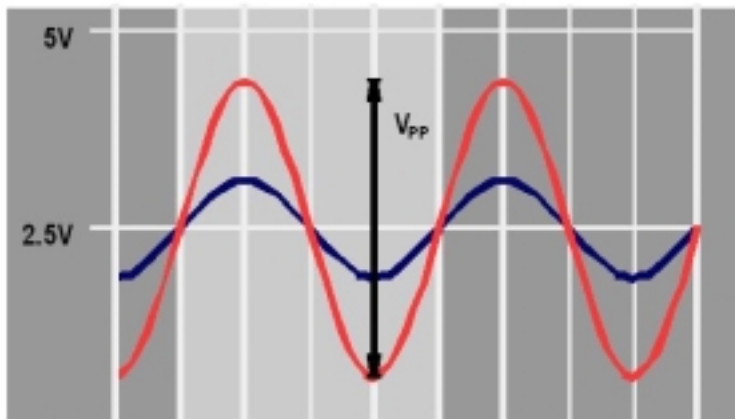


Fig. 1: Measured Op Amp Output Signal

Measured results are shown in Fig. 2. As expected, for low-frequency signals (in this case, 1 kHz), the THD stays constant as signal amplitude increases. Only when the difference between the output voltage and power-supply rails becomes less than 10 mV can a significant decrease in performance be noticed. As the output signal frequency increases, this voltage difference also increases. For a signal of 10 kHz the performance decrease begins at a voltage difference that is less than 200 mV; for 20 kHz, less than 300 mV, and so on. As frequency increases less output signal swing is available if performance preservation is important.

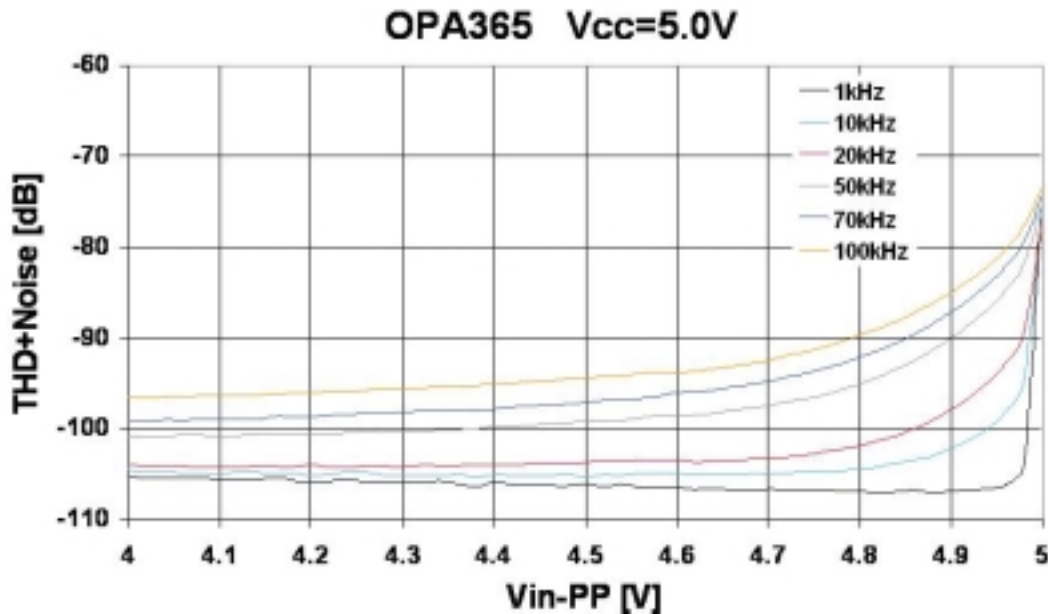


Fig. 2: Measured Op Amp Distortion For Different Output Signals

These results can help us determine an optimum working point for a SAR ADC circuit, considering the output stage limitations of the op amp. For the OPA365 using a 5 V power-supply as in the previous example, an output signal up to 4.1 Vp-p at 150 kHz will preserve its performance. Allowing 450 mV headroom from the power-supply rails, the OPA365 can easily drive signals in the range of 100 kHz.

Influence Of RC Load On The Op Amp

In the previous analysis, we established that for maximum ac performance, the op amp output signal will swing between 450 mV and 4.55 V. The second important parameter of an op amp driving a SAR ADC is to find its limitations in driving different RC loads. As discussed in Part II of this series, it is highly recommended to use an RC filter on the ADC input to limit input noise bandwidth, as well as to assist the op amp with driving the switched capacitive load presented by the SAR ADC. Fig. 3 illustrates the test setup circuit that can help determine the drive limits of the op amp with an RC load.

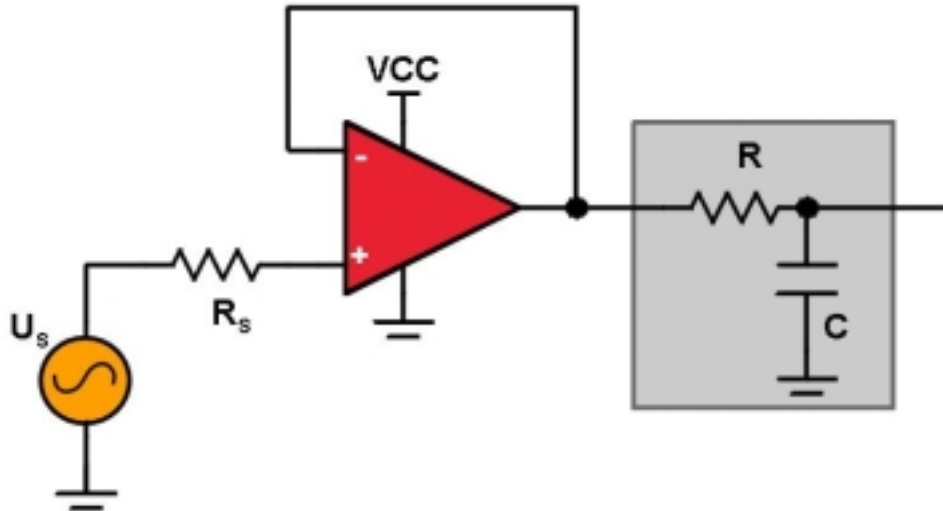


Fig. 3: Measuring Op Amp Capacity To Drive RC Load

As a starting point, a cut-off frequency of 1.5 MHz is selected for the RC circuit. This limit is based on the desired acquisition time of the ADC that will be used later in the design. Keeping the cut-off frequency constant, measurements are done for different RC combinations, as well as different signal frequencies. Fig. 4 shows the measured results.

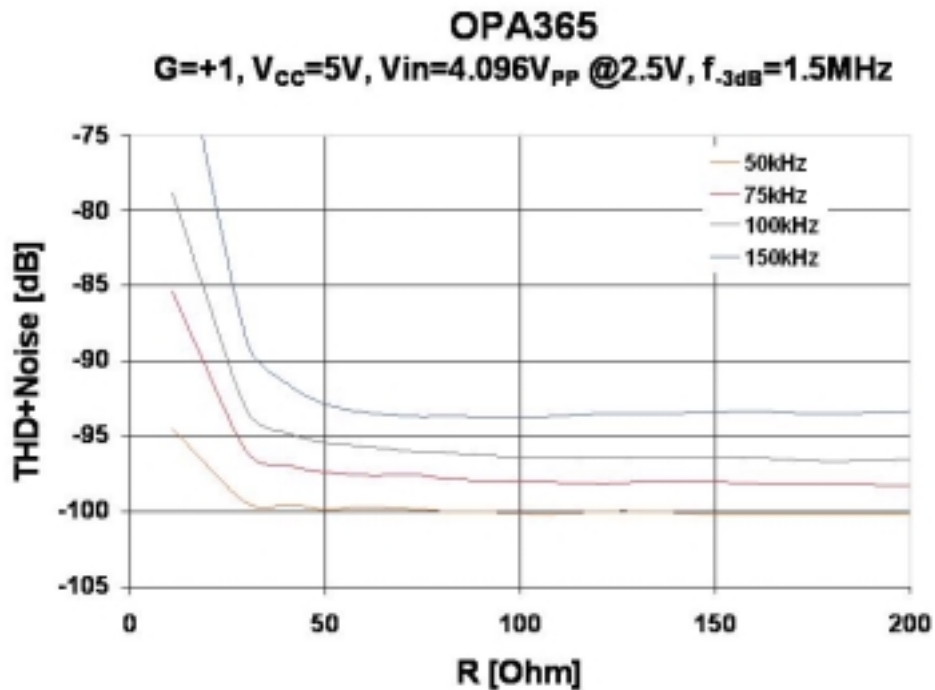


Fig. 4: Measured Op Amp Distortion For Different RCs

You can see from these curves that, for lower frequencies, we can apply a smaller value resistor or a larger capacitor. As signal frequency increases, a larger resistor needs to be used along with a smaller capacitor to preserve performance. For the OPA365 under previously established conditions, we can see that using a resistor value between 50 Ω

and $100\ \Omega$, there is a small improvement – especially for higher signal frequencies. Using a resistor greater than $100\ \Omega$, or capacitor smaller than $1\ \text{nF}$, ac performance stays constant for applied frequency. Observe requirements for stability of the op amp when considering the values of resistors and capacitors [1].

ADC Input Nonlinearity

We have explained, and confirmed with measurements, that reducing output voltage swing helps us preserve the op amp performance. Now, let's look at signal integrity and the impact it has on different components in the system. The next step is to apply a signal to the ADC input. Fig. 5 shows the typical input stage of the SAR ADC. After passing the input electrostatic discharge (ESD) protection diodes, the signal is sampled with a sampling capacitor and two field effect transistor (FET) switches. If ideal components were used, this design will not present any challenge for driving the op amp during the sampling phase.

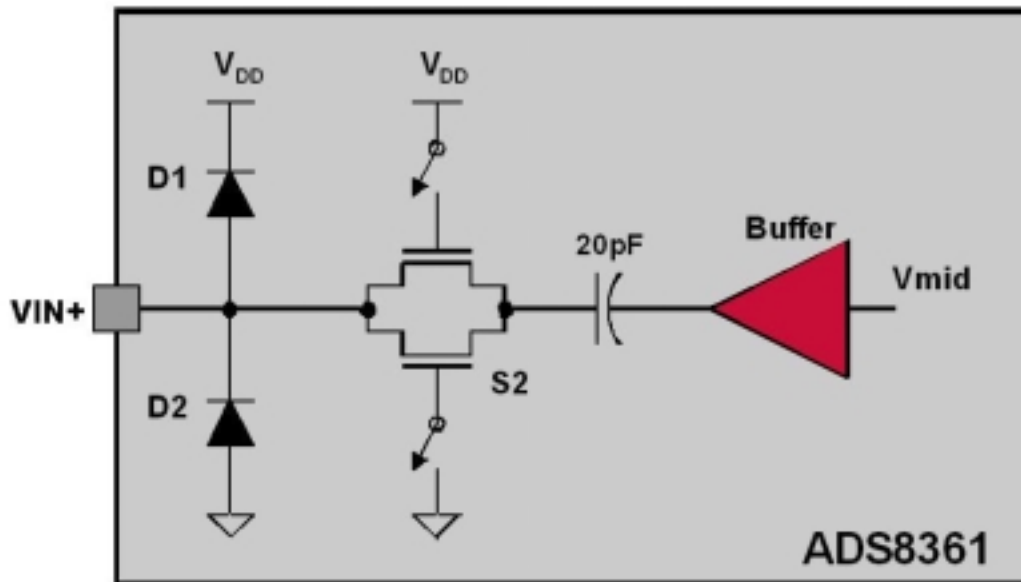


Fig. 5: Representative input stage of a SAR ADC

Unfortunately, these components are not ideal. The equivalent input stage seen by the op amp is shown in Fig. 6. The equivalent load nonlinearity, especially close to the power-supply rails, will present additional challenges for the buffer circuit. In Fig. 12 of Part II the equivalent input impedance as a function of the input voltage is illustrated.

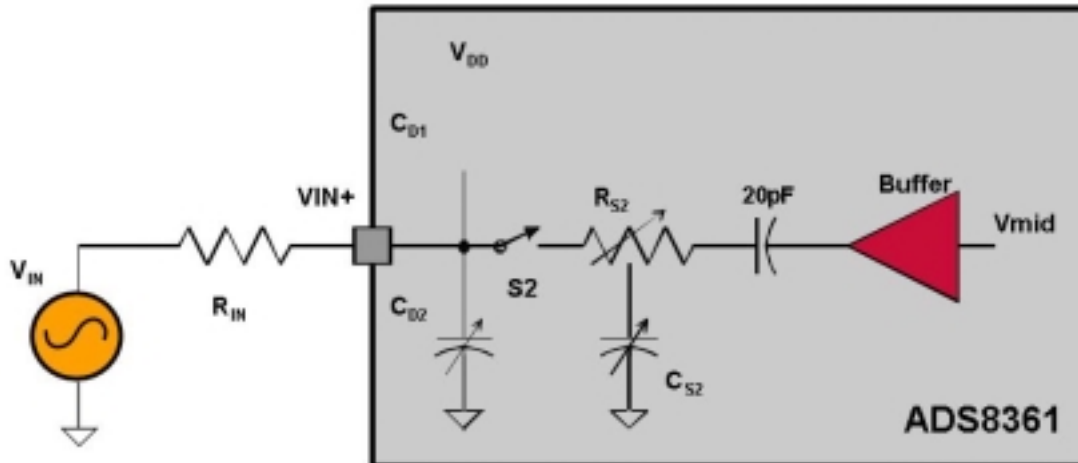


Fig. 6: Equivalent Load To Op Amp Presented By SAR ADC

Reducing the signal swing coming from the op amp and going to the ADC input provides several advantages. If we were trying to use a 5 Vp-p signal on the output of the op amp, THD will be compromised, especially at higher frequencies. Additionally, applying a 5 Vp-p signal to the SAR ADC input requires an op amp with strong drive capability, especially close to the power-supply rails. Reducing the signal from 5 Vp-p to 4.1 Vp-p with a 2.5 V offset adds a margin of 450 mV to both the positive and negative power supply rails. This configuration makes it much easier for the op amp to provide good THD for higher frequencies. At the same time, the equivalent input load of the ADC is in the linear region, making it much easier for the op amp to charge the sampling capacitor.

Loss of the full-scale range of the ADC is another concern. In a typical ADC data sheet, the converter is specified for a rail of 5 V, as well as the full-scale range (FSR) of a 5 Vp-p signal. Keeping in mind that the input FSR of the ADC is determined by the applied reference voltage, it is easy enough to adjust the FSR for the new operating conditions. In the case of a TI ADS8361, when the applied reference voltage is 2.5 V, the FSR input signal will be ± 2.5 V at 2.5 V, or 5 Vp-p. Changing the reference voltage to 2.048 V, the new (adjusted) FSR will be ± 2.048 V at 2.5 V, or 4.1 Vp-p. In this way, we have a full 16-bit conversion on the 4.1 Vp-p input signal without losing dynamic range.

Acquisition Time Versus Throughput Rate

When selecting an ADC, one of the most important parameters is speed, or throughput rate. This parameter is a combination of acquisition time (or sampling time) and conversion time. Conversion time is a consequence of both the converter design and the silicon process used to realize the converter. Reducing conversion time beyond specified data sheet limits seriously corrupts ADC performance. This time is usually specified for the maximum external clock that can be applied. Good system design practice keeps the external clock at the limit or conversion time for as short a period as possible, in line with data sheet specifications. On the other hand, increasing conversion time does not usually provide any increase in performance.

Acquisition time is also specified in the ADC data sheet. This time determines how fast the sampling capacitor must be charged to obtain the specified throughput rate. At the end of the acquisition time, the input sampling switch opens and the conversion process starts. The data obtained from the ADC at the end of the conversion cycle is equivalent to the voltage on the sampling capacitor at the beginning of a conversion cycle (in other words, at the end of the acquisition cycle). Fig. 7 shows the complete process.

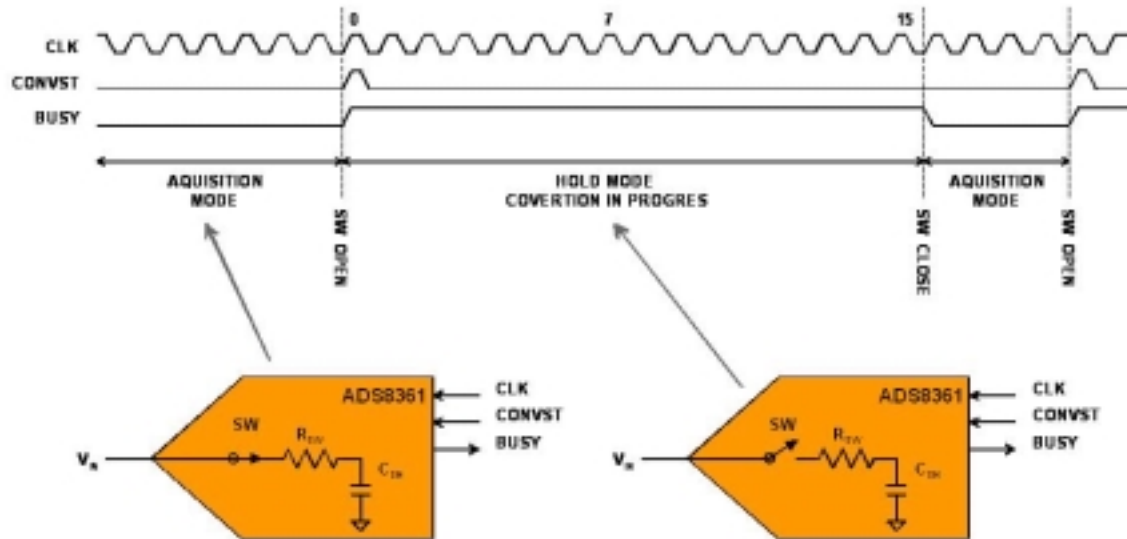


Fig. 7: ADC Acquisition And Conversion Cycle

No matter how well an ADC performs, if there is not enough time provided to properly charge the sampling capacitor, the conversion results will not correspond to the actual analog input signal. To keep this parameter under control, during system design, two different approaches can be taken. One approach is to use a faster op amp with lower output impedance, as well as using a higher cut-off frequency in the RC filter on the ADC analog input. This method can lead to stability problems with the op amp and a higher noise contribution of the input analog buffer circuit. A second method is to increase the converter acquisition time, permitting the use of moderate speed op amps as well as having a lower cut-off frequency of the RC filter.

The ADS8361 has a throughput rate of 500 ksample/s with a maximum external clock frequency of 10 MHz. The conversion process takes 16 clock cycles, or 1.6 μ s. These two numbers leave only 0.4 μ s for acquisition of the analog input signal. In a 16-bit system with a full-scale range of 5 V, the input sampling capacitor of the ADC needs to be charged to the input signal level with an error that is less than 38 μ V. This task is a challenging one for the driving op amp: to settle in 400 ns to less than 38 μ V of the final value.

This issue can be alleviated by increasing acquisition time. For the ADS8361, the specified conversion time is four times longer than the acquisition time. Increasing the acquisition time by a factor of three, (300%), we can obtain 70% of the maximum converter throughput, or 357 ksample/s. This decrease in speed may be a small price to

pay compared to the benefits realized in relaxed requirements for the input signal buffering circuit. Table 1 shows the increase in acquisition time and corresponding decrease in throughput rate for the ADS8361 as a function of the number of external clock cycles.

NxCik	t_{AQ}		Throughput Rate	
	[μ s]		[kSPS]	
4	0.4	100%	500	100%
5	0.5	125%	476	95%
6	0.6	150%	455	91%
7	0.7	175%	435	87%
8	0.8	200%	417	83%
9	0.9	225%	400	80%
10	1	250%	385	77%
11	1.1	275%	370	74%
12	1.2	300%	357	71%
13	1.3	325%	345	69%
14	1.4	350%	333	67%
15	1.5	375%	323	65%
16	1.6	400%	313	63%
17	1.7	425%	303	61%
18	1.8	450%	294	59%
19	1.9	475%	286	57%

Table 1: Throughput Rate As A Function Of Acquisition Time

Optimizing RC For Specific Frequency Performance

From the previous parts of this TechNote [2, 3], as well as the preceding discussion, the procedure for designing the drive circuitry can be derived. First, consider op amps that suit your system power rails, keeping in mind the input and output limitations of such amplifiers, and possibly modifying the ADC input range to better match the op amp capabilities. Second, determine the appropriate acquisition time and set your system timing accordingly. Next, choose the values of the RC circuit. As discussed in Part II the ratio (k) between acquisition time and the time constant of the RC filter depends on the ADC resolution. Finally, choose an op amp with sufficient gain-bandwidth to drive this RC circuit and one with an appropriate settling time. This procedure has proven very robust over many different applications of SAR converters. However, in many cases it is merely a starting point; we have observed that at times, some optimization of the RC filter can be done to improve the performance of a system.

As an example, consider optimizing the circuits discussed previously. Before exploring the optimization of the input RC filter in front of the ADS8361, we need to specify the working conditions. For example, an input clock of 9.9968 MHz is applied and a sampling frequency of 199.936 ksample/s was set.

As the consequence of these two numbers, the conversion time of the ADC is 1.6 μ s, and the sampling (or acquisition) time is 3.4 μ s. Then, for this 16-bit converter, we require that 12 time-constants of the external RC filter fit into the acquisition time. This

condition sets the bandwidth of the RC circuit to:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R \cdot C} = \frac{1}{2 \cdot \pi \cdot \frac{t_{AQ}}{k}}$$

where, $k = 12$. This result leads to a bandwidth of 562 kHz.

Experience tells us that for a low-noise system we should use as much bandwidth as needed but no more, because wider bandwidths permit more noise to enter the system. There must be a balance between the RC settling time and this bandwidth – but does our design using the k values shown previously achieve this?

To determine the best value for the RC filter, we used a signal source with low output impedance. Fig. 8 shows the test set-up used for the measurements.

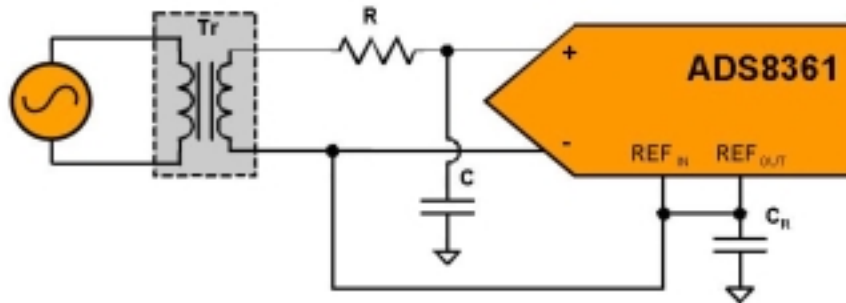


Fig. 8: RC Filter Selection Using Ideal Signal Source

Using this setup, the measurement results are not affected by the input buffer. In the final calculation it is important to include the output impedance of the signal source; in our case, this impedance was 20 Ω . Measurement results are shown in Figs. 9 and 10.

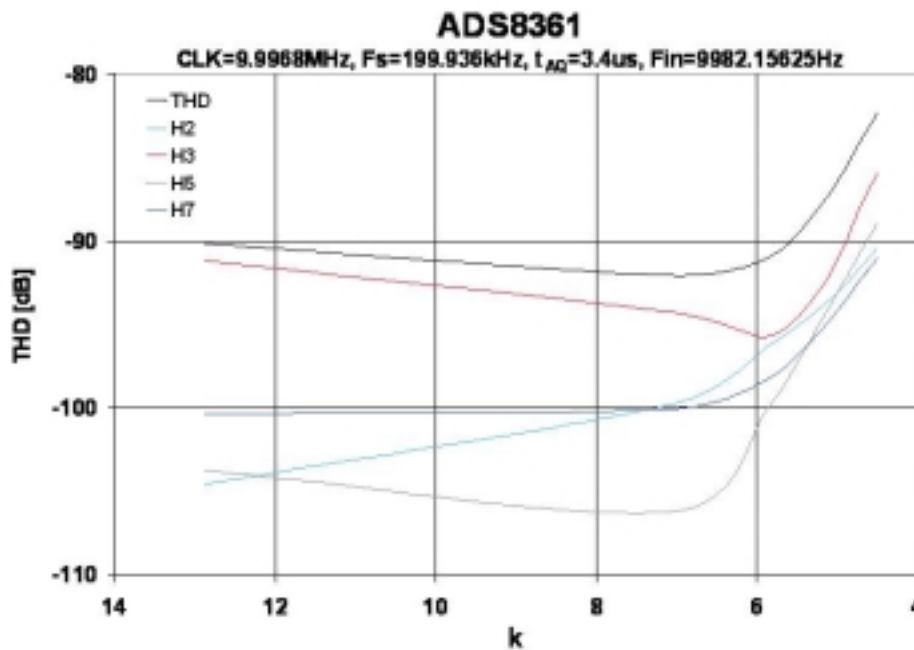


Fig. 9: Measured THD For Different RC Constants

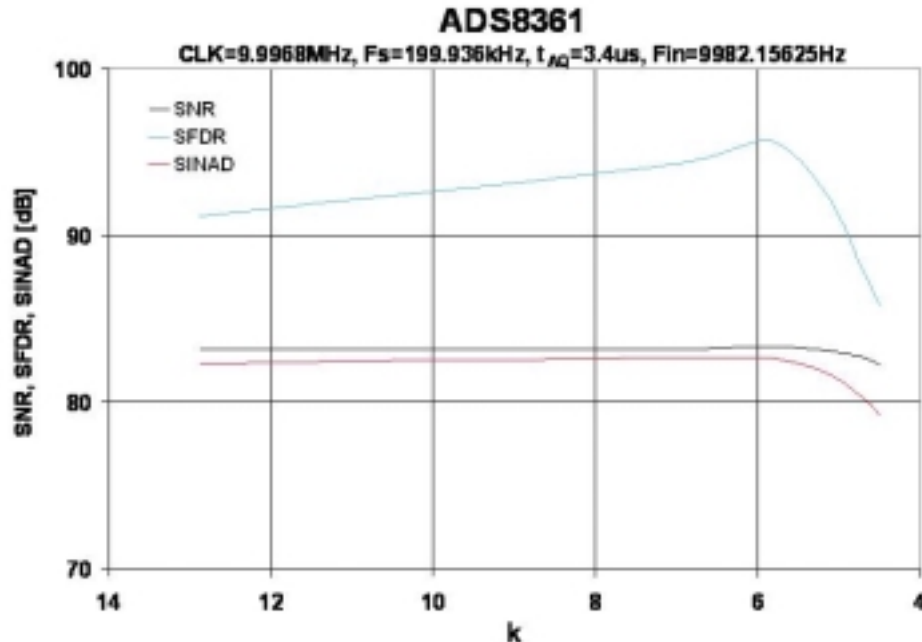


Fig. 10: Measured SNR/SFDR/SINAD For Different RC Constants

From these measurements we can see that the best THD is obtained when $k = 7$, while the best SFDR is obtained when $k = 6$. Intuitively these results make some sense, because lower values of k will cause the bandwidth of the RC filter to be decreased and thereby limit noise. However, for smaller k , we will see performance degradation because the time constant is too long and does not permit proper settling of the input voltage on the sampling capacitor, resulting in a measurement error.

We also see that the performance difference between the procedure-chosen and the optimized values is about 2 - 3 dB. Depending upon the application this difference may, or may not, be significant. Why is there a discrepancy between the design procedure and the optimized results? The design procedure assumes the worst-case conditions for charging the ADC input sampling capacitor, and thus gives the most conservative values for settling time; optimizing by testing often finds that the operating conditions of the circuit are not worst-case, and that some of the assumptions used in determining the design procedure need to be modified. This will be explored in a future TechNote.

Results

For the final performance evaluation of the signal chain, our choice of the RC filter is based on using $k = 6.36$, or a 298 kHz cut-off frequency. That result led us to use a 2.2 nF COG-type capacitor and a 243 Ω resistor. Slowing down the ADC by making the acquisition time longer has an additional advantage: the cut-off frequency of the filter limits the effective noise bandwidth of the input signal to the ADC, or output from the operational amplifier.

When the maximum ADC sampling speed is used, the acquisition time will be 400 ns. Using the same criteria as before ($k = 6.36$) gives us an effective noise bandwidth of 4 MHz for the first-order filter.

$$BW_n = \frac{1.57}{2 \cdot \pi \cdot \frac{t_{AQ}}{k}} = \frac{1.57}{2 \cdot \pi \cdot R \cdot C}$$

$$BW_n = \frac{1.57}{2 \cdot \pi \cdot \frac{400ns}{6.36}} = 3.975 MHz$$

In our example, as the acquisition time was extended from 400 ns to 3.4 μ s, the effective noise bandwidth was reduced to 562 kHz.

For selecting the configuration and component values, we use the results of the previous measurements. Fig. 11 shows the final setup.

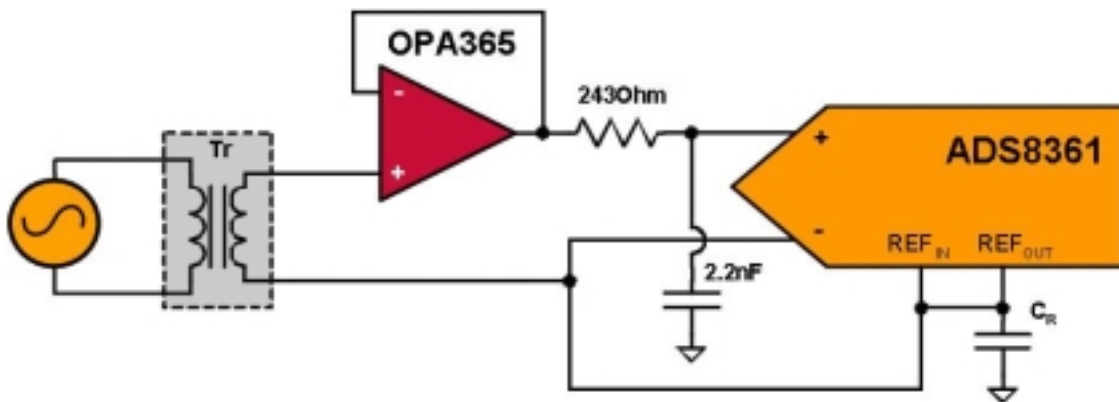


Fig. 11: Final Measurement Setup

Comparing measurements gives us an idea how valuable this procedure can be when designing the signal chain. As a reference point we use values from the ADS8361 data sheet. Next, we compare results obtained from our tests with the selected RC filter in front of the ADC. From Table 2 we see there is THD performance degradation that we can attribute to the signal source used for this experiment (it was clearly not the same signal source used to characterize the ADS8361). The final comparison is with the measurements taken from the complete solution: an OPA365 with RC filter and an ADS8361.

	SNR	SINAD	SFDR	THD	ENOB
ADS8361 DS	83.0	83.0	94.0	-94.0	13.50
RC+ADS8361	83.1	82.2	93.5	-89.1	13.35
OPA365+RC+ADS8361	83.4	82.6	94.1	-90.4	13.42

Table 2: Comparison Of Final Measurements

From these results, we can conclude that a properly-designed buffer circuit in front of the ADC converter does not degrade system performance. Fig. 12 shows an FFT measurement of the complete system.

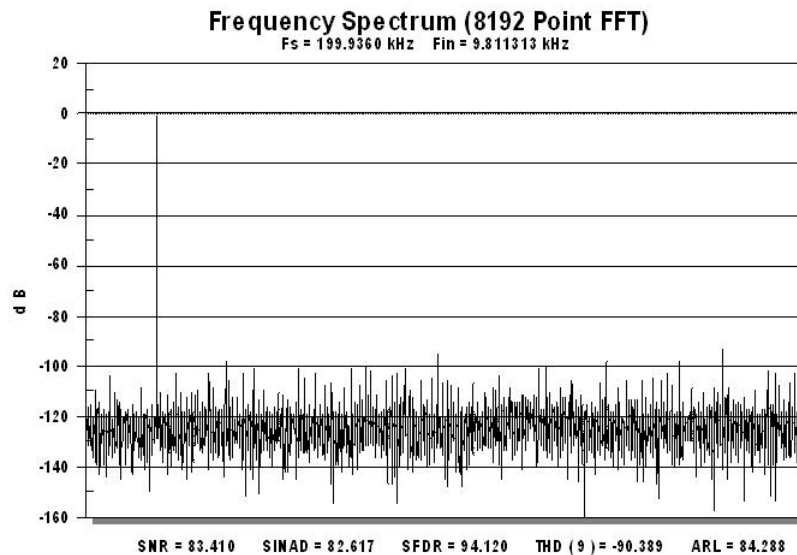


Fig. 12: Measurement Results Of Complete Signal Chain

Conclusions

Together with the previous two parts of this TechNote, we introduced a procedure for designing drive circuitry for SAR-type ADCs. In doing so, we focused on the op amp requirements and some of the techniques that can be used to optimize the op amp and ADC system. Slight changes to the ADC timing make all the difference to an application. Furthermore, we discussed some further optimizations to the RC circuit in front of the SAR, but these performance tweaks are very application-specific and need careful consideration. From these results, we conclude that a properly-designed buffer circuit in front of the ADC converter will not degrade system performance.

References

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