

Analog-To-Digital Converters Part 2 Of 6: Do I Need All My Bits

by Bonnie C Baker and Russell Anderson, Texas Instruments Incorporated

Using Extra Converter Bits for Analog Gain

Temperature is the most widely measured phenomena in the process control environment. Circuit designers use common sensing elements such as resistance temperature detectors (RTDs), thermistors, thermocouples, or diodes to sense absolute temperatures. Of these technologies, the platinum RTD (PRTD) temperature sensing resistive element is the most accurate and stable over time and temperature. Although the RTD temperature sensor may be an accurate choice for your application needs, the element's sensitivity and low resistance presents challenges when bringing the sensor's signal conditioning chain to the controller.

Many temperature applications require digital results that are just one part out of 4000. You can obtain this level of granularity with a 12-bit converter, because a 12-bit converter conveniently produces 4096 or 2^{12} possible code combinations. Prior to the ADC the translation from sensor resistance to voltage requires a gain and an anti-aliasing filter stage. You can implement both of these stages with analog circuitry prior to the 12-bit SAR ADC (see Fig. 1a). An alternative solution is to implement these functions with digital circuitry inside a 24-bit, delta-sigma ($\Delta\Sigma$) ADC (see Fig. 1b).

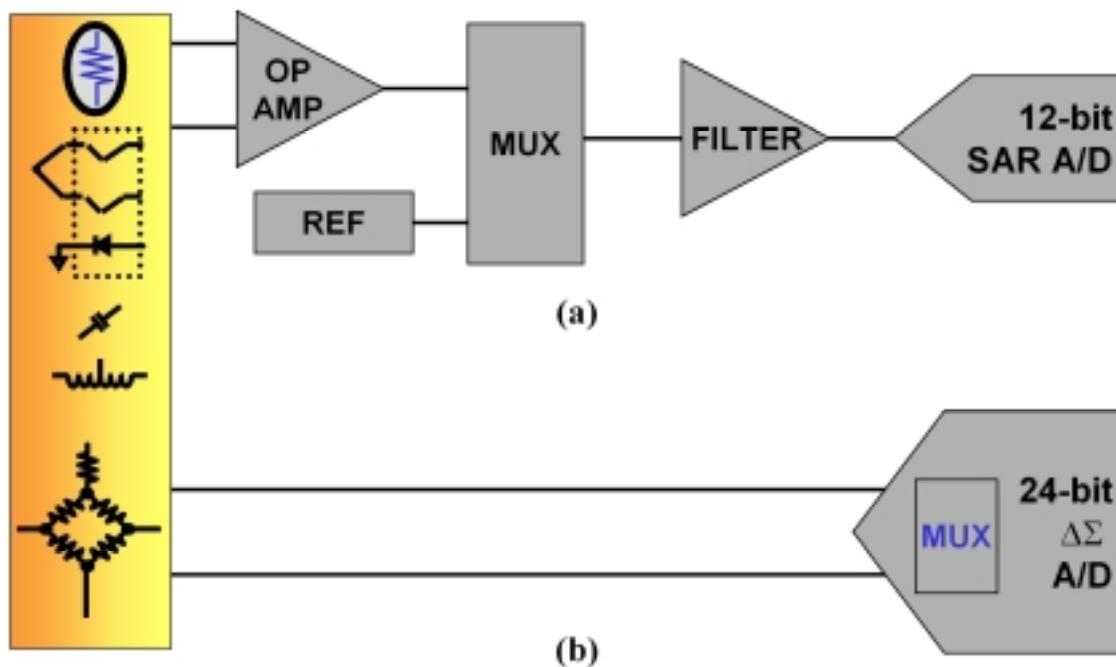


Fig. 1: Digitizing the RTD Sensor Signal this Circuit Uses an Analog Gain Stage Followed By a Multi-Order Anti-Aliasing Filter and 12-Bit SAR ADC

The Resistance Temperature Detector

The most stable, linear and repeatable RTD is made of platinum metal. The temperature coefficient of the RTD element is positive. You can calculate an approximation of the platinum RTD absolute resistance change over temperature by using the constant $0.00385 \Omega/\Omega/^\circ\text{C}$.

$$\text{PRTD}(T_A) = \text{PRTD}_0 + T_A \times \text{PRTD}_0 \times 0.00385 \Omega/\Omega/^\circ\text{C}$$
where, $\text{PRTD}(T_A)$ is the resistance value of the platinum RTD sensing element at temperature (Celsius)
 PRTD_0 is the specified resistance of the PRTD element at 0°C (Ω)
 T_A is the ambient temperature around the PRTD element (Celsius)

The RTD element resistance is low. Typically, specified 0°C values for RTDs are 50, 100, 200, 500, 1000 or 2000 Ω . Of these options, the 100 Ω platinum RTD is the most stable over time and linear over temperature. If the RTD element is excited with a current reference at a level that does not create an error due to self-heating, the accuracy of this sensing element can be $\pm 4.3^\circ\text{C}$ over its entire temperature range of -200°C to $+800^\circ\text{C}$. If a higher accuracy temperature measurement is required, you can use a look-up table or the linearity formula below (Calendar-Van Dusen Equation).

$$\text{RTD}(T_A) = \text{RTD}_0 (1 + AT_A + BT_A^2 - (100CT_A^3 + CT_A^4))$$
where, A, B, and C are constants derived from resistance measurements at 0°C , 100°C and 260°C

The RTD element requires a current excitation. If the magnitude of the current source is too high, the element will dissipate power and start to self-heat. Consequently, a good design ensures that the sensor excitation current is less than or equal to 1 mA.

Designing an RTD 12-bit ADC System

The circuit in Fig. 2 effectively converts the variable resistance value of the RTD sensor to a 12-bit digital word. The evaluation of this circuit starts with the 2.5 V precision voltage reference (A_5 , upper right corner). A_5 connects directly to R_{11} . Since the non-inverting input of the CMOS amplifier, A_1 , is high impedance, the voltage drop across R_{11} and R_{12} is equal. The voltage is equal at the inverting and non-inverting input of A_1 . The formula $1 + (R_{14} \div R_{13})$ gains inverting input voltage to the output of the amplifier and the top of the reference resistor, R_{15} . Voltage at the output of A_1 is equal to:

$$V_{\text{OUTA1}} = (1 + (R_{14} \div R_{13})) * (V_{15} - V_{R11}) = 2 * (V_{15} - V_{R11})$$
where, V_{OUTA1} is the voltage at the output of A_1 ,
 V_{R11} is the voltage drop across R_{11} ,
 V_{R15} is the voltage across the reference resistor

If $R_{13} = R_{14}$, the voltage at the output of A_2 is equal to $V_{15} - 2V_{R11}$. This same voltage appears at the inverting input of A_2 and across to the non-inverting input of A_2 .

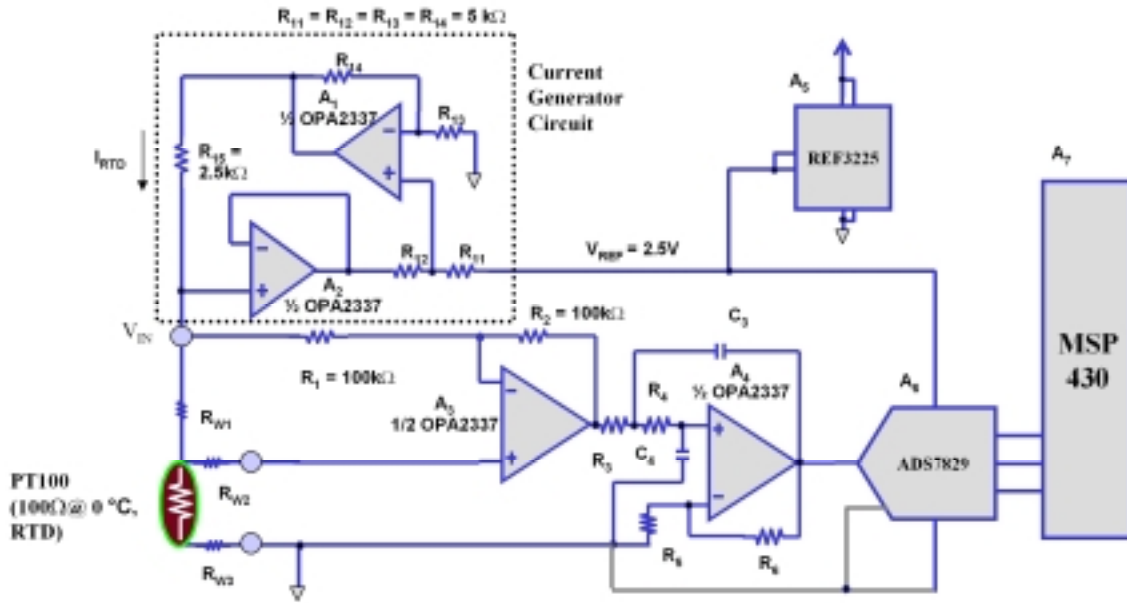


Fig. 2: Digitizing the RTD Sensor Signal this Circuit Uses an Analog Gain Stage Followed by a Multi-Order Anti-Aliasing Filter and 12-Bit SAR ADC

Solving these equations, the voltage drop across the reference resistor, R_{15} is equal to:

$$\begin{aligned}
 V_{R15} &= V_{OUTA1} - V_{OUTA2} \\
 &= 2 * (V_{15} - V_{R11}) - (V_{15} - 2V_{R11}) \\
 &= V_{15}
 \end{aligned}$$

The current through R_{15} is equal to:

$$I_{RTD} = V_{R15} \div R_{15}$$

This circuit generates a dc, floating, current-source that is ratiometric to the voltage reference and the ADC.

Absolute errors in the circuit will occur as a consequence of the absolute voltage of the reference, the initial offset voltages of the op amps, the output swing of A_1 , mismatches between the resistors (R_{11} , R_{12} , R_{13} , and R_{14}), the absolute resistance value of R_{15} , and the RTD element. Errors due to temperature changes in the circuit will occur as a consequence of the temperature drift of the same elements listed above. The primary error sources over temperature are the voltage reference (A_5), offset drift of the op amps (A_1 and A_2), and the RTD element.

RTD Signal Conditioning Path Using the SAR ADC

In the circuit using a SAR converter (Fig. 2, again), the RTD element equals $100\ \Omega$ at 0°C . If the RTD senses temperature over a range from -200 to $+600^\circ\text{C}$, the range of resistance from the RTD is nominally $23\ \Omega$ to $331\ \Omega$. Since the RTD resistance range is relatively low, wire-resistance and wire-resistance change-over-temperature can skew the measurement of the RTD element. The three-wire RTD device reduces these errors.

The op amp A_3 removes the wire-resistance error of R_{W1} and R_{W3} . In this configuration, R_1 and R_2 are equal and relatively high. Select the value of R_1 to ensure that the leakage currents through the resistors do not introduce errors to the RTD element. The transfer function of this portion of the circuit is:

$$V_{\text{OUT:A3}} = (V_{\text{IN}} - V_{W1})(1 + R_2 \div R_1) - V_{\text{IN}}(R_2 \div R_1)$$

where,

$$V_{\text{IN}} = V_{W1} + V_{\text{RTD}} + V_{W3},$$

V_{Wx} is the voltage drop across the wire to and from the RTD,
 $V_{\text{OUT:A3}}$ is the voltage at the output of A_3

If $R_1 = R_2$ and $R_{W1} = R_{W3}$, the equation above reduces to:

$$V_{\text{OUT:A3}} = (V_{\text{RTD}} + V_{W3}) (2) - (V_{\text{RTD}} + 2V_{W3})$$
$$V_{\text{OUT:A3}} = V_{\text{RTD}}$$

A second-order, low-pass filter, removes higher frequency noise from the voltage signal at the output of A_3 . This filter is built using A_4 , R_3 , C_3 , R_4 , and C_4 . The resistors R_5 and R_6 also gain the analog signal by $75\ \text{V/V}$. The low-pass filter in this circuit should have a cut-off frequency that is as low as possible reducing amplifier and conducted noise. Choose the Chebychev filter (0.5 dB ripple) because of its fast transition region in the frequency domain. The closest expected high frequency noise in this circuit is 60 Hz. The attenuation of this filter at 60 Hz is 39 dB down from dc. The noise from the CMOS amplifiers could be as high as $29\ \text{nV}/\sqrt{\text{Hz}}$ (rms) @ 10 kHz. The noise due to the two amplifiers in the circuit signal path will be $48\ \mu\text{V}$ (rms) or $0.318\ \text{mV}_{(\text{p-p})}$ at the input to the 12-bit, ADC. With a 10 Hz, second-order Chebychev filter only $\sim 2\ \mu\text{V}$ (p-p) remain in the signal. More critically, the noise that is injected by the mains frequency (50 Hz or 60 Hz) is reduced by -24.5 dB or -27.9 dB. This is equal to an attenuation of 16.8x or 23x.

The LSB size of the 12-bit converter is equal to:

$$\text{ADC}_{\text{LSB}} = V_{\text{REF}} \div 2^{12}$$
$$= 2.5\ \text{V} \div 4096$$
$$= 0.610\ \text{mV}$$

The sample speed of the SAR ADC can be as slow, or as fast, as need be. Your selection of this sampling speed will not affect the accuracy of the conversion.

The SAR ADC is a good fit to this type of application. Be willing to carefully gain the voltage from the resistive RTD, but the gain cells are easy to implement. The biggest challenge in this circuit is the current reference circuit. The SAR converter offers a low-power, low-cost solution that is easy to implement.

Defining a New Approach

Delta-sigma ADCs have an innate ability to resolve an analog input signal to a very small LSB voltage size. At first glance, high resolution doesn't seem to be an important specification for the RTD temperature sensor, as long as you use an analog gain stage. However, by using a converter with high resolution, an analog gain stage is not needed. Even if the signal only uses a portion of the input range of the 24-bit converter, it can have more resolution and a smaller LSB size than a 12-bit ADC that includes external gain. The sensing element's output could be in the hundreds of millivolts, but the output voltages that represent a change in temperature can be extremely low (sub-mV or $-\mu\text{V}$). If the dynamic resolution of the ADC alone is relatively high, the total device count is reduced by removing the front-end gain stage and reducing the complexity of the anti-aliasing filter (see Fig. 3).

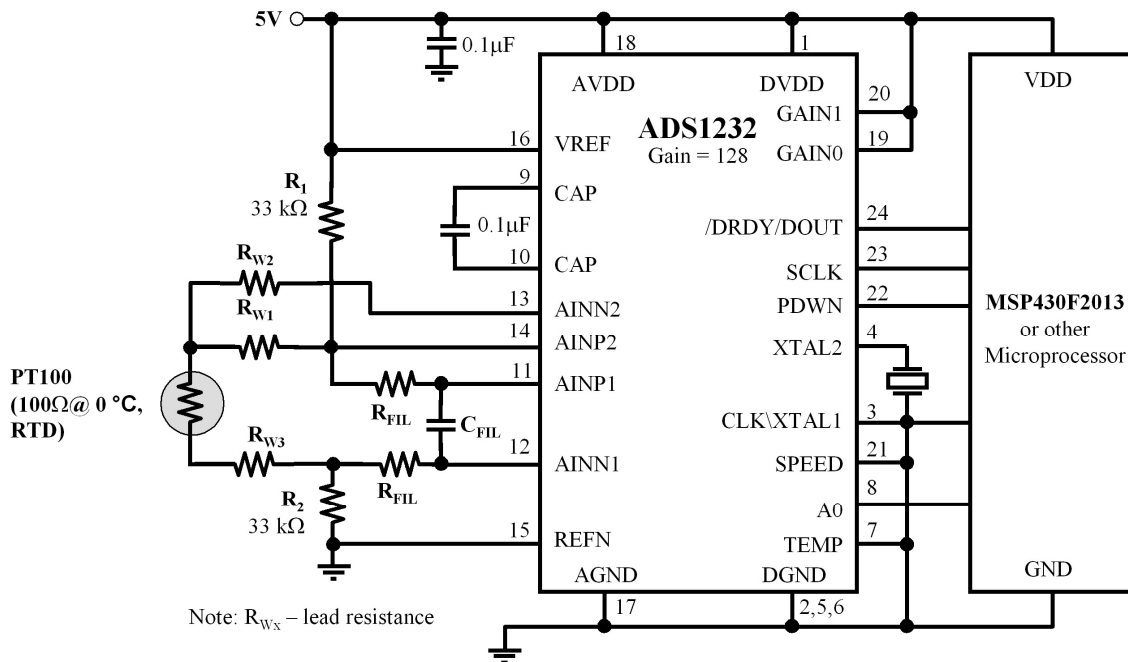


Fig. 3: Alternative to 12-Bit SAR ADC Uses 24-Bit Delta-Sigma Converter and Analog Input Gain Stage

For the given RTD of $100\ \Omega$ (@ 0°C) with an excitation current of $80\ \mu\text{A}$, the nominal full-scale output voltage range (-200°C to $+600^\circ\text{C}$) would be $29.48\ \text{mV}$. The digitizing system that follows the RTD should reliably represent the temperature to 12-bit accuracy (given the error contributions of the RTD). The designer can choose to gain and actively filter the RTD voltage using analog techniques and many parts (at a higher cost) or put a digital engine to work: the delta-sigma converter, which makes this precision application possible because of its superior digital processing.

The circuit in Fig. 3 combines a high precision, three-wire lead PRTD with the ADS1232 $\Delta\Sigma$ ADC from Texas Instruments. Here, R_1 and R_2 in series with the power supply excite the RTD as well as establish the common-mode voltage of the ADS1232 programmable

gain amplifier (PGA). This circuit uses both of the ADS1232 differential channels. You eliminate the temperature change in lead resistance, R_{WX} by using the following formula:
$$(AINP1 - AINN1) - 2(AINP2 - AINN2)$$

This calculation assumes that $R_{W1} = R_{W3}$. If the wires to each PRTD pin are the same length and made of the same material, this is a good assumption.

The internal $\Delta\Sigma$ noise reduction techniques improve the performance of the circuit. The data rate of the converter is 10 Hz (as programmed) to reduce interference from the mains (50 Hz or 60 Hz) frequency. A simple R-C filter can be used to remove the possibility of aliasing from the 76.8 kHz sampling frequency. This low-frequency data rate is possible because of the slow responsiveness of the RTD element to temperature. The conversion noise level of the ADS1232 is 17 nVrms. This equates to 22.1 usable bits or 19.3 noise free bits. The LSB size of this converter using PGA = 128 is 2.3 nV or 0.000064°C. This is much more resolution than we need, and means that we can actually ignore or discard some of our extra resolution.

If the layout is good, you can select a subset of the possible bits. Out of the 2^{24} possible data results, there are 32 sub-regions. Each of those regions has 17 bits of resolution. This extra resolution is why you eliminate the gain stage of the SAR converter circuit (Fig. 3, again). The sample rate of this type of converter matches the sensor and the physical event. Since this converter will give you a high number of noise-free-bits, you can ignore the ones that don't fit into your range of interest and still get a 12-bit conversion out of the deal.

Selecting *Sweet Bits* Out of 24-bit Conversion

You may be right about the output resolution of your system, but wrong about the actual resolution that you require from your converter. Many applications require digital results that are just one part out of about ~4000. You can obtain this level of granularity with a 12-bit converter, because a 12-bit converter conveniently produces 4096 or 2^{12} possible code combinations. This type of converter seems like a perfect fit to your application woes. Once you select your 12-bit ADC converter, you can go about designing the complete system. The ADS7829, 12-bit converter, might fit the bill.

But, step back and consider thinking about the actual input system LSB size. This may change your perspective enough, making the 12-bit converter only an alternative instead of a requirement. If you keep your eyes on the objective and use the system specifications as a guide, you may find that a 24-bit delta-sigma converter provides the right solution.

Reference

A Baker's Dozen: Real Analog Solutions for Digital Designers by Bonnie Baker, Newnes-Elsevier, 2005

About The Authors

Bonnie Baker is a Senior Applications Engineer for Texas Instruments in Tucson, Arizona, and has been involved with analog and digital designs and systems for nearly 20 years. In addition to her fascination with circuit design, Bonnie has a drive to share her knowledge and experience and has written over 250 articles, design notes, and application notes. Bonnie Baker is the author of *A Baker's Dozen: Real Analog Solutions for Digital Designers* (Newnes, 2005). You can reach her at bonnie@ti.com

Russell Anderson is a Senior Applications Engineer for Texas Instruments Data Acquisition Products group in Tucson and specializes in microsystem converters. He earned a BS at Brigham Young University in Provo, Utah. Anderson can be reached at anderson_russ@ti.com

