

circuit. The oscillator output is short pulses that are inverted for a logic high most of the time. The inverted pulse both clocks the 74AHCT76 counter and turns off Q4, allowing diode D3 to conduct the current from the source including Q5. R11, D2, R13 forms a temperature-compensated voltage divider that sets a voltage on the base of Q5. Its emitter resistance, R2, R12 then sets the current that charges C3, C4 to a new voltage step level. R2 adjusts the current and sets the step height or amplitude.

Meanwhile, the counter chain of 4 JK flops counts down by 16 as a ripple counter, then clocks Q3 through C2. Q3 turns on and discharges the staircase capacitors. Just as the PUT can be replaced by two transistors, or even a 555 timer, the counter can be replaced by 74HCT74 flops instead, or by one four-stage binary or decade counter IC of the 7400 series. The two polypropylene capacitors can likewise be replaced by a single, cheap 2.2 μ F ceramic capacitor.

The Q6, Q7 JFET buffer of matched transistors can also be eliminated by using a JFET input dual op amp such as the TL072CP. The op amp buffer drives an inverting amplifier to invert and reduce in amplitude the staircase waveform, the size of which can be adjusted by the amplitude calibration pot. Finally, the output also drives two VCOs (U7) to provide 1 MHz and 10 MHz frequency-modulated outputs. The MC4024 dual VCO (not to be confused with the 4000-series CMOS logic family) is also a legacy part that can better be replaced with a 4000-series CMOS VCO such as the 4046 or 74HCT4046 (moved from the 4000 series into 7400 series).

The circuit, as given, was originally designed in August 1973 for use in Tektronix demonstrations of products at trade shows, where an interesting waveform was needed for the scope or spectrum analyzer displays. The staircase generator is simple enough -- a gated current source into a capacitor which is discharged by a transistor -- that a μ C implementation is nowadays a minimal parts-count solution. Use two bit output lines, for current-source gating and staircase reset, and retain the current source and output op-amp(s) for buffering and scaling. Calibrate the staircase height by using a [simple \$\mu\$ C ADC](#) to adjust the current source on-time duration, the frequency by setting an interrupt timer with the desired value, and the number of steps with a timer-driven counting loop.

With VCO, the unit could be used as a spectrum analyzer tracking generator, for generating frequency markers. It could also be applied to test scanning transceivers, where the stairsteps are calibrated to be at channel frequencies. Stairsteps are also found in the vertical interval test signal (VITS) of NTSC video waveforms and in curve tracers, for stepping base or gate drive as a parameter for each of the current-voltage curves.

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