Electronics Quiz # 2

by Dennis L Feucht

Electronics Quiz # 1, given earlier in TechNotes, might have been too easy for some of you hot-shot engineers. Now here is a quiz that will not only provide somewhat more of a challenge but also possibly give you some new insights.

The Motor Torque Control Problem

An engineer is designing a fan control circuit and is having some trouble with the motor, which is overheating. The fan uses the usual square-law blades, where torque increases by the square of the speed. The fan is designed to run at 3600 rpm, where the motor is operated at its maximum power. The motor torque is proportional to motor current, controlled by sensing it with a sense resistor. When the system is turned on after being off a long time, it runs normally at 3600 rpm, but then the speed decreases as the motor heats up, from an ambient 25°C at turn-on to 75°C. The engineer has measured the stall torque and noticed that it falls off at the higher temperature to 80% of what it was at 25°C. What is the fan speed at the higher temperature and what basic error in design is the engineer likely to have made? You may refer to COMEX (Commodities Exchange) data to establish your conclusion, if necessary.

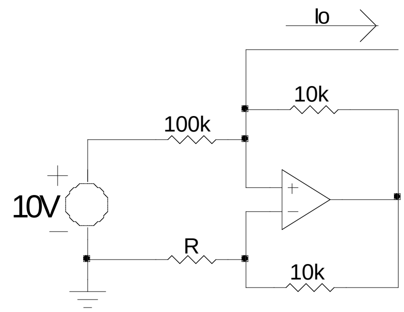
ANSWER

This happened to the author, years ago, in designing an automotive blower motor controller. A low-resistance sense resistor was needed and in an attempt to save money, a short length of copper wire was used for it. Copper has a fractional TC of TC% = 0.4%/°C near ambient temperature. Over 75°C – 25°C = 50°C, the change in resistance was $(0.4 \times 10^{-2}/°C)\cdot(50°C)$ or 20%. At 1.2 times its 25°C value and with the same circuit threshold voltage, the current was reduced by about 20% and the torque with it. At 0.8 times the torque, the speed is lower by $\sqrt{0.8} \approx 0.894$, or about 19% below the nominal speed, or 3218 rpm.

The solution? A more experienced power engineer took me over to ESI, the instrument company known for RLC meters, where he worked previously, and had one of the people on the assembly line cut me some lengths of manganin wire, a low TC alloy good for making sense resistors. I got some #16 AWG wire made by the Wm B Driver Co, with 0.381 Ω/m or 3.81 mΩ/cm, formed a half-loop of it with a length of about 3 cm, tinned the ends, soldered it into the board, and the problem was solved.

Copper sense resistors can be used to advantage, however, as a low-cost form of temperature foldback limiting. The diameter of copper wire can be varied to set its self-heating to where a desired reduction in current with temperature occurs. COMEX data is, of course, entirely irrelevant to the problem.

The Op Amp Current Source



The above circuit is intended to be a current source. What must the value of R be for the output resistance to become infinite? What is the value of the output current?

ANSWER

If R = 100 kΩ, then not only is the circuit symmetrical but any change in circuit (not op amp) output voltage, v_o, which is at the noninverting input, v_+, of the op-amp, will change the op amp output voltage by v_o·(10 kΩ/100 kΩ + 1). This change at the op amp output, when divided down by the top divider to v_+ will be equal to v_o, thus bootstrapping the voltage change and keeping the output current unchanged.

More rigorously, let the op amp output voltage change be v_A. Then applying the noninverting op amp voltage gain:

$$v_A = \left(\frac{R_f}{R_i} + 1\right) \cdot v_o$$

Then summing the output current change at the output node as a result of v_o:

$$i_o = -\frac{v_o}{R_i} - \frac{v_o - v_A}{R_f} = -v_o \cdot \left(\frac{1}{R_f} + \frac{1}{R_i}\right) + \frac{v_A}{R_f}$$

$$= -\frac{v_o}{R_i \parallel R_f} + \left(\frac{R_f}{R_i} + 1\right) \cdot \frac{v_o}{R_f} = -\frac{v_o}{R_i \parallel R_f} + \left(\frac{R_f + R_i}{R_i \cdot R_f}\right) \cdot v_o$$

$$= \frac{v_o}{R_i \parallel R_f} \cdot (-1 + 1) = 0$$

No change in output current, i_o, occurs, which is what is expected of a current source.

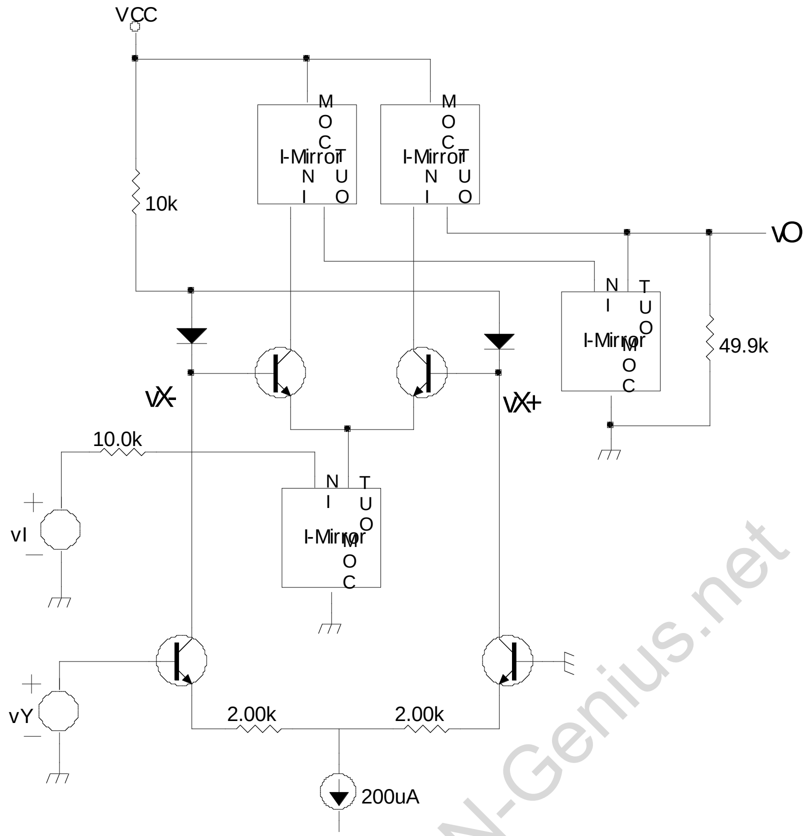
The value of static output current follows from the above equations in their static form. We could omit V_R above because it is unchanging, but for static calculation we put it in. Then applying KCL at the output node:

$$I_O = \frac{V_R - V_O}{R_i} + \frac{V_A - V_O}{R_f} = \frac{V_R}{R_i} - \frac{V_O}{R_i \parallel R_f} + \frac{V_A}{R_f}$$

$$= \frac{V_R}{R_i} - \frac{V_O}{R_i \parallel R_f} + \frac{V_O}{R_i \parallel R_f} = \frac{V_R}{R_i}$$

Substituting, I_O = (10 V)/(100 kΩ) = 100 μA.

Variable-Gain Amplifier



The VGA shown above is a somewhat idealized depiction of a two-quadrant translinear multiplier. The core of it could be implemented with a CA3080 or half of a LM13600 or LM13700. The diodes and BJT *b-e* junctions are matched and have the same area. The input voltage is v_I, and output voltage is v_O. The gain is varied by input v_Y. Find the voltage gain:

$$A_v = \frac{v_O}{v_I}$$

What is the value of v_Y for $A_v = ½$?

ANSWER

The upper pair of matched BJTs with diodes shunting their bases and driven by the lower pair of BJTs is a classic translinear gain cell. The collector currents of the upper BJT pair will have a ratio equal to the lower pair. The collector currents of the lower pair are (close to) linearly related to v_Y in that one will have a current of $x \cdot 200$ μA and the other of $(1 - x) \cdot 200$ μA. Their ratio will be duplicated in the upper BJT pair. The left BJT current is mirrored twice and appears as negative (sinking) current at the output. The right BJT is mirrored once and its current is positive (sourced).

For $v_Y = 0$ V, $x = 0.5$ and the lower current source is equally split between BJTs at 100 μA each. For $v_Y = 0.4$ V, $x \approx 1$ and all the current is in the left transistors. For $v_Y = -0.4$ V, $x \approx 0$, and the right transistors have it all.

The input voltage creates an input current in the series R of 10 kΩ which is replicated in the current mirror and split between the upper BJT pair according to x. For equal currents (x = 0.5), the algebraic sum at the output is zero and the gain is zero. For the extremes of v_Y, all of one or the other currents of the pair become output current, and the output voltage is about:

$$v_O \approx (\pm v_I/10.0\ \text{k}\Omega)\cdot(49.9\ \text{k}\Omega)$$

Then the extreme values of the voltage gain are:

$$A_v \approx \pm\frac{49.9\ \text{k}\Omega}{10.0\ \text{k}\Omega} = \pm 5$$

More generally, for a given v_Y, the bottom pair of BJTs produces:

$$x = \frac{1}{2}\cdot\left(\frac{v_Y}{0.4\ \text{V}} + 1\right)$$

The upper BJTs amplify by:

$$A_v = \frac{v_O}{v_I} = \frac{R_O}{R_I}\cdot(1-2\cdot x) \approx 5\cdot(1-2\cdot x)$$

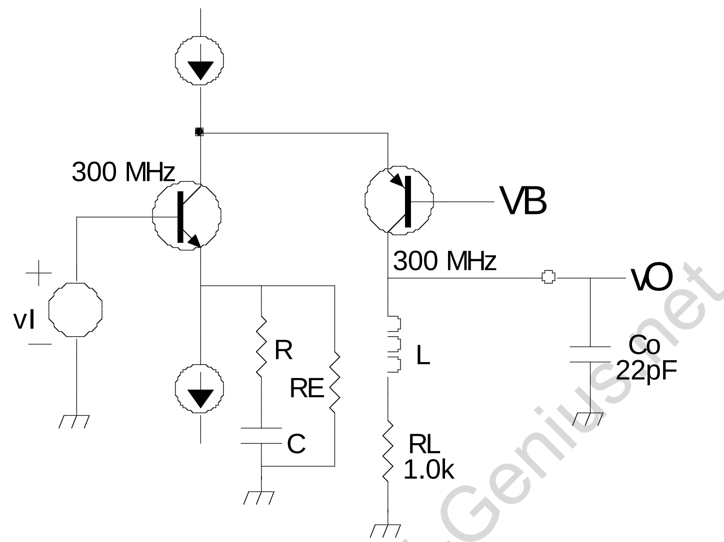
Given the way the output current mirrors are wired, a positive gain is effected by negative values of v_Y. For a gain of +0.5, then solving for v_Y from the above equations, $x \approx 0.45$, and $v_Y = (-0.1)\cdot(0.4\ \text{V}) = -40$ mV.

For a more accurate rendition of this circuit, an op amp is added to each lower BJT, making the circuit an op amp V/I converter. Similarly, a V/I converter is used to drive the upper BJT pair source current-mirror input so that the mirror input current is exactly v_I/R_I.

The 10 kΩ resistor that terminates the 200 μA source circuit at the diode anodes drops 2 V, enough to allow the high-side mirrors to operate linearly. The mirrors themselves can be implemented as Wilson current mirrors. Or simply two matched transistors – pnp for the high-side and npn for the low-side mirrors – would also be sufficient for applications where the gain and offset are nulled out by either hardware or software adjustment.

Fast Complementary Cascode Amplifier

Finally, for those not sufficiently challenged by the above problems, your high-speed amplifier acumen is now placed under some scrutiny with this problem. The complementary cascade voltage amplifier stage, shown below, uses transistors with an f_T = 300 MHz, such as the familiar 2N3904 and 2N3906 BJTs. What value of *L*, used to peak the output frequency response, will result in an approximately maximally-flat envelope delay (MFED or Butterworth) response and have a pole angle of 30°? By what factor is the bandwidth extended relative to the same circuit without the inductance (*L* = 0 H)?



ANSWER

The MFED response is only approximate because shunt peaking (unlike series peaking) has an additional zero in the response. This makes it somewhat faster and less damped. If we take the approach of using *L* to compensate for the bandwidth reduction caused by the 22 pF load capacitance, then for a 30° pole angle, the damping is:

$$\zeta = \cos(30°) \approx 0.866$$

Damping can also be expressed using the quantity more familiar from communications theory:

$$Q = \frac{1}{2 \cdot \zeta} \approx 0.577$$

For shunt peaking:

$$\zeta = \frac{1}{2 \cdot \omega_n \cdot (L / R_L)}$$

where, R_L = 1.0 kΩ and:

$$\omega_n = \frac{1}{\sqrt{L \cdot C_o}}$$

As given, C_o = 22 pF. Solving the two equations for *L*:

$$L = (Q \cdot R_L)^2 \cdot C_o = \frac{R_L^2 \cdot C_o}{4 \cdot \zeta^2} = \frac{(1.0\ \text{k}\Omega)^2 \cdot (22\ \text{pF})}{4 \cdot (0.866)^2} = 7.33\ \text{ìH}$$

Then $f_n = \omega_n/2\cdot\pi$ = 12.53 MHz. The bandwidth extension factor is 1.881 times $1/R_L\cdot C_o = 2\cdot\pi\cdot$(7.234 MHz), and the bandwidth is $1.086\cdot\omega_n$. Using either bandwidth calculation:

(1.881)·(7.234 MHz) = (1.086)·(12.53 MHz) = 13.61 MHz

A more penetrating problem would have also asked what R and C compensate and what their values should be. They provide *emitter peaking* as an alternative in compensating the output pole of R_L and C_o by introducing a pole and zero into the response. The zero (at $1/R\cdot C$) is set to cancel the output pole and the remaining pole (of $1/(R||R_E||r_e)\cdot C$) is at a higher frequency than the cancelled output pole, thereby extending bandwidth.

Not included either are the BJT effects in the *high-frequency region*, between $f_\beta = f_T/\beta_o$ and f_T. For a nominal quasistatic (low-frequency ac) β_o = 150, the h_f range is 2 MHz to 300 MHz. In this range, the amplifier input impedance is no longer a simple $(\beta_o + 1)\cdot(r_e + R_E)$. At the base, R_E is gyrated into a series RC with series $R = R_E$ and series $C = 1/2\cdot\pi\cdot f_T\cdot R_E$. Any source resistance would form an impedance divider with the gyrated base resistance, possibly leading to another use for the emitter peaking circuit.

For a more complete answer and development of wideband amplifier theory and practice, refer to my book, *Designing High-Performance Amplifiers* http://www.scitechpublishing.com volume three of a four-volume set on analog circuit design.