

Practical Design of a Buck Converter

Part 1: Buck Converter Design

by Dennis L Feucht

The purpose of this design mini-course is to take those familiar with analog circuit design, but not power electronics, through the detailed design of a very common type of switching power converter as an example.

A *converter* is a dc-dc power supply. The term *dc* is ambiguous meaning either *unipolar* or *constant*. For converters, it generally means unipolar, and often means constant too. For line-operated inputs, the familiar rectifier and storage capacitor can be used to provide unregulated input dc. Some low-power converters, such as the ICL7660, use switched-capacitor circuits for conversion, but they cannot store energy as densely as magnetic materials and are useful only at low power: here we will use magnetics for higher power.

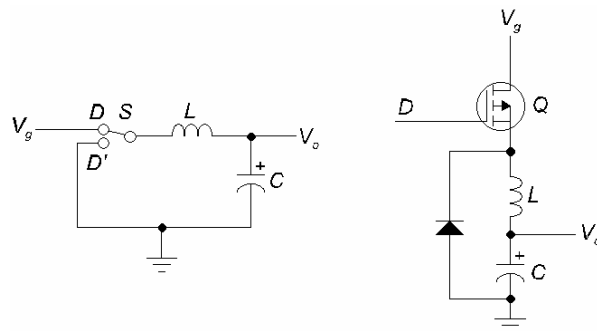
Inefficient linear supplies have been steadily replaced by switchers with efficiencies of 75% to 95%. A linear supply is, basically, a dc power amplifier and a technology well within the realm of analog circuit design. A switching supply introduces a nonlinear device, the converter power switch. Like the transistor, it is three-terminal and can be linearized around its operating-point parameter: the duty ratio, D . Richard Tymerski developed the incremental (or small-signal) switch model for control analysis which will be introduced here.

Another complication to switched circuits is that sampling theory must be applied for accurate analysis. Ray Ridley discovered that pulse-width modulation (PWM) in converters effects a kind of current sampling which he subsequently analyzed and modeled. For converter control, the feedback loop must include a *sampling gain* block for accurate analysis. Besides these nonlinear functional blocks, the others are familiar to the analog engineer.

A design procedure for a buck regulator will be developed here, a step at a time. Although the design formulas are not difficult to use, knowing how they were derived is critical to development of design reasoning about their application and also insight into power circuits.

Buck Converter Circuit Explained

The figure below is that of a *buck (common-passive) converter* circuit, used when $V_g > V_o$. A common feature of basic switching converters is the single-pole, double throw switch, S , in series with the inductor, L .



For a buck converter, the switch is at the input. In a practical circuit, as shown, the MOSFET transistor is the active on-time switch, and the diode is the passive off-time switch which conducts when the MOSFET is off. When switch S is on, current from V_g increases through L , charging C and supplying current to the load connected across V_o . The inductor current reaches a maximum when S switches off. The current in an inductor cannot change instantaneously (just as the voltage across a capacitor cannot). Consequently, when S switches off, the inductor current will then flow from ground, through the diode and into the inductor. The current is now opposed by the voltage across L , which is now more positive at the V_o terminal. The current

decreases and C will discharge when the load current exceeds the inductor current. The charging and discharging of C causes voltage variation, an *ac* voltage component or *ripple*, at the output. At the end of the switching cycle, S switches on and the sequence repeats.

To design a buck converter, we need to determine component values. These are calculated from design formulas that we derive from basic circuit theory. The values we substitute into the formulas are the design goals (or *criteria*) that we want to achieve, such as output voltage and current capability, and maximum output voltage ripple.

Derivation of Design Formulas

S is switched between position D (at V_g) to D' (ground) by control circuits (not shown). The fraction of the switching period that the switch is in position D (or on) is the *duty ratio* (or duty cycle):

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T_s} = 1 - D'$$

where, t_{on} and t_{off} are the *on-* and *off-times* of S . The total (on + off) time is the switching period, T_s . The output voltage is controlled by controlling D .

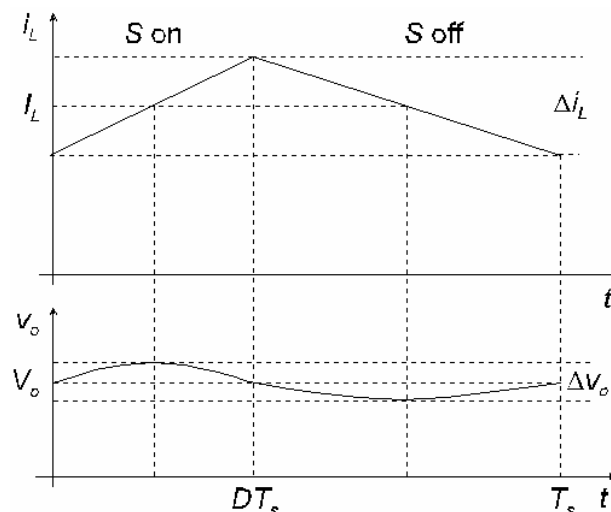
When S is on, the input voltage is applied to the input side of the inductor, L . Under normal operation the capacitor is charged to the desired output voltage, V_o . The voltage across L is then $V_g - V_o$. The rate of change (or slope) of the current in the inductor is:

$$\frac{v_L}{L} \cong \frac{\Delta i_L}{\Delta t}$$

where, the change in inductor current, Δi_L , and Δt are small.

Applied to the inductor of the buck circuit:

$$\frac{V_g - V_o}{L} \cong \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{t_{on}}$$



With S on, i_L increases (because $\Delta i_L/\Delta t > 0$), as shown above.

S turns off at time $D \cdot T_s$, when inductor and switch current is maximal. This peak current value is a factor in the current rating for both the MOSFET and diode.

Derivation of Output Voltage

The converter steady-state transfer function, V_o/V_g is controlled by D and can be derived by equating Δi_L of the on- and off-times. If a constant average current in the inductor is maintained (that is, steady-state operation), then over the switching cycle, Δi_L must equal zero if the average current is to stay the same. Solving

$$\frac{v_L}{L} \cong \frac{\Delta i_L}{\Delta t}$$

for Δi_L and applying it to the on-time, the change in current is:

$$\Delta i_L(\text{on}) = \frac{(V_g - V_o) \cdot (D \cdot T_s)}{L}$$

The off-time is the remainder of the switching period after the on-time, or:

$$t_{\text{off}} = T_s - D \cdot T_s = (1 - D) \cdot T_s = D' \cdot T_s$$

During the off-time, the inductor current change is:

$$\Delta i_L(\text{off}) = -\frac{(-V_o) \cdot ((1 - D) \cdot T_s)}{L}$$

Then for no change in I_L , $\Delta i_L(\text{on}) = -\Delta i_L(\text{off})$, and

$$\frac{(V_g - V_o) \cdot (D \cdot T_s)}{L} = \frac{V_o \cdot ((1 - D) \cdot T_s)}{L}$$

Solving for the transfer function, we get:

$$\frac{V_o}{V_g} = D$$

The output voltage is simply proportional to D and V_g .

Derivation of Output Voltage Ripple

The designer chooses the desired values of V_g and V_o and maximum output current, along with the amount of output ripple voltage, Δv_o , that can be tolerated. Given these design criteria, component values can be calculated from design equations we will now derive.

First, note in the above graphs that the current ramps up and down, producing a triangle-wave ac component of current. The average value of i_L is centered between maximum (or peak) and minimum current values and is also the average output current:

$$\bar{i}_L = I_o = \hat{i}_L - \Delta i / 2$$

The average current is midway between the peak current value, \hat{i}_L , and minimum (or valley) value.

Next, the varying (or ac) output voltage across C , v_o , follows this triangle-wave of current with some phase lag according to the capacitor v - i relationship:

$$\frac{i_C}{C} \cong \frac{\Delta v_C}{\Delta t}$$

From the above graph for i_L , during the time for which $i_L > I_L$, the change in capacitor voltage is:

$$\Delta v_o \cong \frac{\bar{i}_{L+} \cdot \Delta t}{C}$$

where, \bar{i}_{L+} is the average value of i_L while it is above I_L .

For the upper half of the current-ripple triangle, the average value of i_L is half of $\Delta i_L/2$, or $\Delta i_L/4 + I_L$. For the off-time half-cycle, it is $I_L - \Delta i_L/4$. With I_L amount of current going to the load, this leaves $\Delta i_L/4$ to charge C . v_o reaches its peak halfway through the on-time, at $(D/2) \cdot T_s$. Under steady-state operation, the values of both i_L and v_o are the same at the end and beginning of the switching cycle. The off-time half-cycle therefore must have the same value of \bar{i}_{L+} . We can now find the output ripple by substituting for \bar{i}_{L+} in the above equation for both half-cycles and adding them, resulting in a ripple variation (peak-to-peak) of:

$$\Delta v_o = \frac{(\Delta i_L / 4) \cdot ((D/2) \cdot T_s)}{C} + \frac{(\Delta i_L / 4) \cdot (((1-D)/2) \cdot T_s)}{C} = \frac{\Delta i_L \cdot T_s}{8 \cdot C}$$

The approximations assume that $\Delta v_o \ll V_o$. From this ripple-voltage equation, we can see that ripple varies proportionally with inductor current variation. Output ripple voltage can be expressed in chosen design parameters by solving for Δi_L in:

$$\frac{V_g - V_o}{L} \cong \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{t_{on}}$$

Then Δi_L is:

$$\Delta i_L = \frac{(V_g - V_o) \cdot t_{on}}{L} = \frac{(V_g - V_o) \cdot D \cdot T_s}{L} = \frac{(1 - V_o^2 / V_g) \cdot T_s}{L}$$

Substituting for Δi_L in the design formula for ripple voltage:

$$\text{output ripple voltage} = \Delta v_o = \frac{D \cdot T_s^2 \cdot (V_g - V_o)}{8 \cdot L \cdot C} = \frac{T_s^2}{8 \cdot L \cdot C} \cdot \left(1 - \frac{V_o^2}{V_g}\right)$$

Ripple voltage is decreased by increasing L , C , or V_o or by decreasing V_g or T_s . The switching frequency, $f_s = 1/T_s$, and V_o have the greatest effect.

Design Formulas for L and C

Excitation of magnetic components can cause acoustic noise in the audible frequency range, and switching frequency, f_s , is consequently chosen above 20 kHz. As switching frequencies increase with refinement of the technology, typical values of f_s are from 40 kHz to 1 MHz. A higher f_s value will reduce the values for L and C , resulting in smaller converter volume and cost. The upper limit is determined primarily by magnetic core loss. The broad optimum f_s for present-day magnetic cores is around 200 kHz to 400 kHz.

Design formulas for L and C can be derived from previous equations:

$$\Delta i_L \cong \frac{V_L}{L} \cdot \Delta t$$

This equation shows that Δi_L decreases with increasing L . L is chosen to limit Δi_L for a desired peak current, \hat{i}_L , used as a minimum value for component current rating. By solving for L in the ripple-voltage equation:

$$L = \frac{D \cdot T_s^2 \cdot (V_g - V_o)}{8 \cdot \Delta v_o \cdot C} = \frac{T_s^2}{8 \cdot \Delta v_o \cdot C} \cdot \left(1 - \frac{V_o^2}{V_g}\right)$$

Substituting:

$$\Delta v_o = \frac{(\Delta i_L / 2) \cdot T_s}{4 \cdot C} = \frac{(\hat{i}_L - I_o) \cdot T_s}{4 \cdot C}$$

What results is a formula for L expressed only in given design parameters:

$$L = \frac{T_s}{2 \cdot (\hat{i}_L - I_o)} \cdot \left(1 - \frac{V_o^2}{V_g}\right)$$

The design formula for C is then chosen to meet the ripple-voltage requirement. Solving the ripple equation:

$$C = \frac{T_s^2}{8 \cdot L \cdot \Delta v_o} \cdot \left(1 - \frac{V_o^2}{V_g}\right)$$

The output capacitor is often an aluminum electrolytic type. In converters with switching frequencies above 200 kHz, the value is small enough for a multilayer ceramic type to be used instead. Ceramic capacitors have lower series inductance (if the leads are kept short or eliminated by using a surface-mount package) and they can behave as capacitors to these higher frequencies.

Before a capacitor can be chosen, the capacitor rms current must be known. The rms current is used to calculate the power dissipated in the capacitor series resistance, and capacitor current ratings are given in rms current values. For a continuous triangle-wave waveform, $x(t)$, the rms value is:

$$\tilde{x} = \frac{\hat{x}}{\sqrt{3}} = \frac{\Delta x / 2}{\sqrt{3}}$$

Applying Δi_L ,

$$\tilde{i}_C = \frac{\Delta i_L / 2}{\sqrt{3}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(1 - V_o^2 / V_g) \cdot T_s}{L}$$

From this value, an output capacitor can be selected from catalogs. Compromise of L and C values results in minimal component size and cost. As L increases, ripple current decreases, allowing C to decrease. This optimization is best done with inductor and capacitor catalogs in hand. Layout can also be a factor in how this compromise goes, as the size and shape of larger or smaller parts affect board size and part placement.

