Practical Design of a Buck Converter
Part 2: Buck Converter Design
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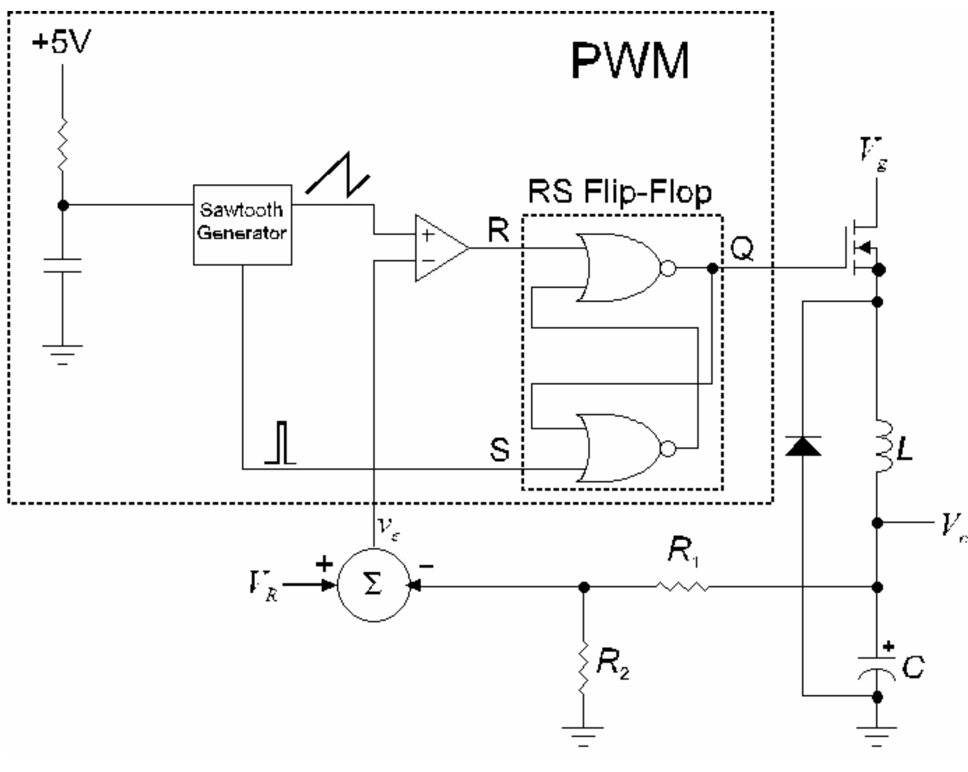
Controller Design

We have completed derivation of the design formulas for the power switching part of the converter. Output voltage regulation is achieved by the controller. It inputs V_o and outputs D. V_o is scaled with a resistive divider, then compared to a commanded value. For fixed-voltage converters, this is a stable and accurate reference voltage. If V_o is low, D is increased; if high, D is decreased.

Various IC controllers are commercially available. Two classic low-cost 8-pin ICs that are useful for reference designs are the UCC3842 and the NE5561 (or variants). Newer parts typically have smaller packages, more features and performance, and a higher price. In choosing a controller IC for long-term use, it is best to select one that has won a long-term reputation in the market and will continue to be available in future years. For short-term designs, any commercially available IC that can be bought in lifetime volumes is also a possibility.

Voltage Control

The functional block of a controller is the *pulse-width modulator* (PWM), as shown in the converter circuit below.



The supply output voltage, V_o, is divided by R_1, R_2 and compared to a reference voltage, V_R. The difference is the regulator feedback-loop error voltage, v_e. The PWM outputs a fixed-frequency pulse from the Q output of the RS flop with a duration that is controlled by its input voltage, the error voltage v_e. The PWM then converts this voltage to a pulse stream with duty ratio, D. This control scheme is called *voltage* (or *voltage-mode*) *control*.

The PWM circuit consists of a sawtooth generator, comparator and RS flop. The sawtooth waveform down-slope is steep, to minimize the minimum *D* and maximize the maximum *D*. During the sawtooth descent, the generator asserts a reset pulse to the S input of the flop. The high level of this pulse sets the flop and turns the MOSFET on, starting a new cycle after the R input becomes low. Then the sawtooth ramps up until it reaches v_e:

$$v_e = V_R - v_o \cdot \left(\frac{R_2}{R_1 + R_2} \right)$$

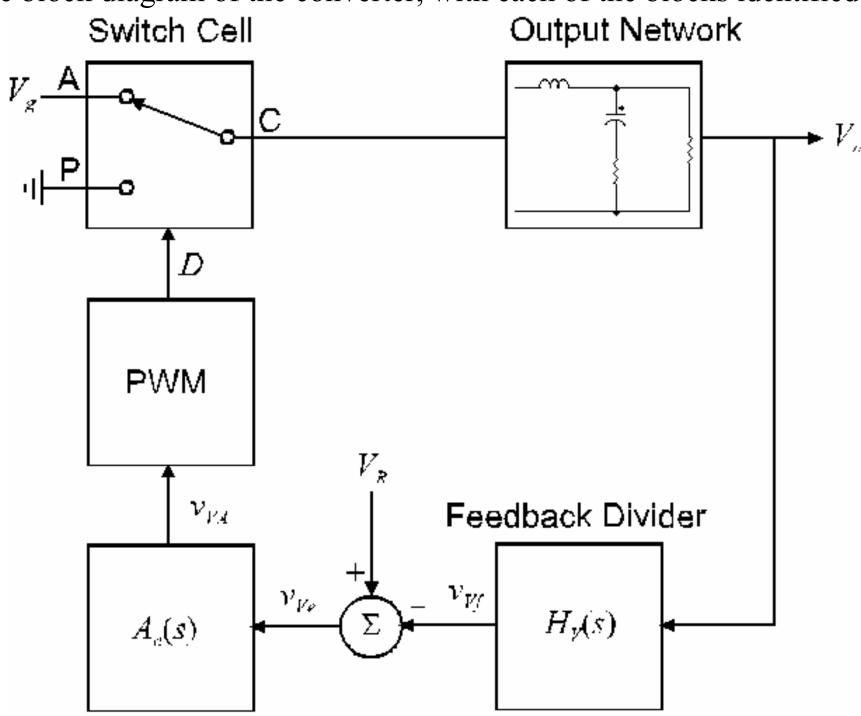
The time from the assertion of the flop Q output to when v_e equals the ramp voltage is the on-time, t_{on}. When the comparator voltages cross, the comparator output asserts high, resetting the flop. Q goes low, the MOSFET switches off, and off-time begins.

V_R is output from a stable and accurate reference source such as a bandgap or Zener reference that is often less than V_o and requires the resistive divider. The summing function is typically the differential input of an op amp, which also provides loop gain and dynamic-response compensation.

As v_o increases, v_e decreases, causing *D* to decrease. Then the cycle-averaged voltage applied to the input side of *L* decreases. Over a cycle, the average voltage at the MOSFET source is $D \cdot V_g$ and is equal, over many cycles, to V_o.

Converter Block Diagram

We can now draw the block diagram of the converter, with each of the blocks identified.



The error-voltage amplifier, $A_c(s)$, has a static (dc) voltage gain and poles and zeros as needed to dynamically compensate or stabilize the feedback loop. These are determined after the loop gain has been derived from the contributions of the other blocks. In the simple voltage controller circuit shown previously, $A_c(s) = 1$ and $v_{VA} = v_e$. This controller has no dynamic compensation and probably insufficient loop gain for accurate regulation. To do control analysis, we must first find the transfer functions (*transmittances* or *gains*) for each of the blocks in the loop.

The PWM output/input transfer function is D/v_e. The linear input range of v_e is that of the sawtooth voltage range, V_{PWM}. When $v_e = V_{PWM}$, then $D = 1$. Then D is the fraction, v_e/V_{PWM} and:

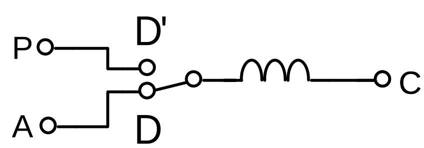
$$\frac{D}{v_e} = \frac{1}{V_{PWM}}$$

For example, the NE5561 has sawtooth extrema of 5.1 V and 1.1 V, or a peak-to-peak value of V_{PWM} = 4.5 V. Its transmittance is therefore 1/4.5 V.

The power-conversion circuit has a steady-state transfer function of V_o/D. The basic circuit *switch* cell within it is the DPDT switch in series with the inductor, or the. An incremental (small-signal) model for the cell has been derived by Richard Tymerski. http://www.innovatia.com/Design_Center/tymerski_switch_model.htm Its circuit model is derived in the next section.

The Switch Mode

In 1986, Richard Tymerski developed an incremental model of a power switch that assumes average currents and voltages during the switching cycle. Vatche Vorperian had discovered that the three basic switching converter topologies were the three possible configurations of a three-terminal device, the inductor in series with a current switch, as shown below.



The switch cell has three terminals labeled P for *passive*, A for *active*, and, C, for the common or *inductor* terminal. The duty ratio is D for the active switch position and $D' = (1 - D)$ for the passive position.

This three-terminal model is reminiscent of the transistor, with its three configurations. Its input and output ports share a common terminal. The common-emitter (CE), common-base (CB), and common-collector (CC) or *emitter-follower* configurations of transistors have analogies with converter power switches. Each of the three switch-cell configurations, based on a common terminal, results in one of the three basic first-order converter topologies.

The switch-cell terminal voltages and currents are averaged over a switching cycle. This limits the applicable frequency range of the switch model to half the switching frequency, which is the *Nyquist frequency*, $f_s/2$. At and above it, aliasing occurs. The switching frequency is the basic parameter affecting allowable system bandwidth, and a model that is valid up to the Nyquist frequency covers the frequency range of interest for linear circuit analysis.

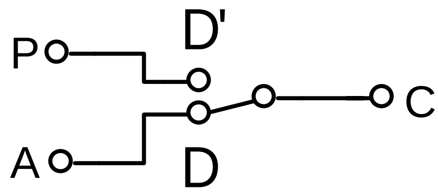
The average inductor voltage over a switching cycle must be zero to maintain flux balance. That is:

$$D \cdot v_{AC} = D' \cdot v_{CP}$$

The notation used here is of the form:

$$v_{XY} = v_X - v_Y$$

With zero average voltage across the inductor, it can be removed from the switch-cell model, which simplifies to the Tymerski switch model, shown below.



When the switch is in the D position, the average voltage from C to P is D times that from A to P, because $v_A = v_C$ during D. That is:

$$v_{CP} = D \cdot v_{AP}$$

Similarly, during the off-time ($D' \cdot T_s$), $v_C = v_P$ and:

$$v_{AC} = D' \cdot v_{AP}$$

For currents, during the on-time ($D \cdot T_s$), the average current into A must equal the average current out of C, or:

$$i_A = D \cdot i_C$$

while during the off-time, while C is connected to terminal P:

$$i_P = D' \cdot i_C = (1 - D) \cdot i_C$$

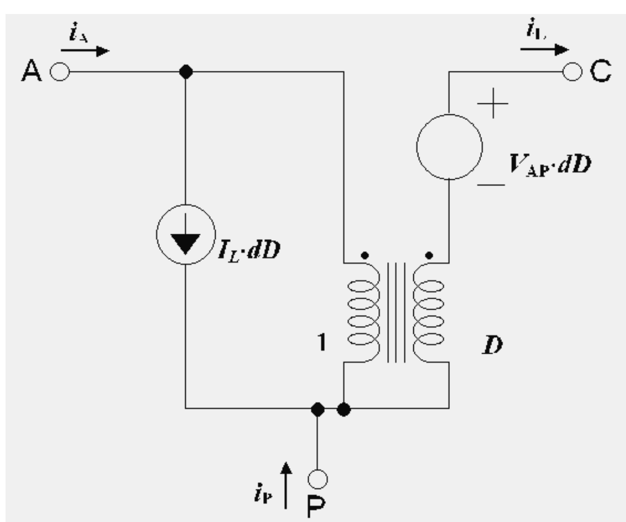
The incremental model of the switch cell can be constructed from these switch-cell equations. Keeping in mind that the symbol, d, is used as the differential of (which is a *small change in*) the following quantity, then incremental duty ratio is dD. Taking the differential of i_A results in:

$$di_A = D \cdot di_C + I_C \cdot dD$$

Applying differential calculus similarly to the other three equations results in the incremental-model equations:

$$di_P = D' \cdot di_C - I_C \cdot dD$$
$$dv_{CP} = D \cdot dv_{AP} + V_{AP} \cdot dD$$
$$dv_{AC} = D' \cdot dv_{AP} - V_{AP} \cdot dD$$

These equations can be expressed in the form of an equivalent circuit, shown below:



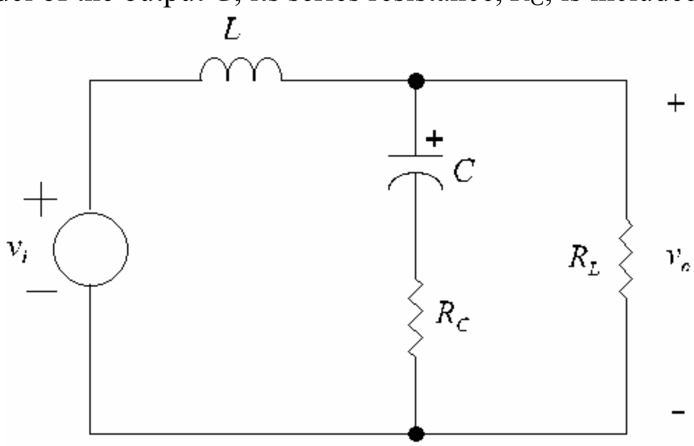
As an incremental model, the operating point is established by the static (dc) model parameters, I_C, V_{AP}, and D. The duty ratio is a large-signal parameter; the model is valid for the nominal value of D of the circuit. Changes around D are dD, the incremental model variable for D. The transformer, with turns ratio of $1{:}D$ or $1/D$, converts voltages and currents by the ratio of D.

This circuit model can now be substituted for the switch in a converter topology, and the dynamic behavior of the circuit derived using the usual linear methods of analog circuit analysis. The series inductor must be included in the circuit model, though it was unnecessary in deriving the switch model under the per-cycle flux-balance assumption. The parameter values are chosen based on the operating point of the circuit. These parameters are readily available from the static design of the converter. Because the switch model is a physical and not a black-box model, it is independent of (and thus unaffected by) the circuit it is placed in.

The assumptions of the model should be remembered: it is valid below the Nyquist frequency ($f_s/2$); it assumes constant values for its three parameters: and assumes inductor flux balance, which is the case in steady-state operation. During start-up and other transient conditions, flux balance is still a reasonable approximation whenever the change in switch parameters is small over a switching period.

Output Network

Another transfer function needed for voltage-control design is the LC output filter, driving a resistive load, R_L. For a more realistic model of the output C, its series resistance, R_C, is included, as shown below.



The transfer function of this circuit can be derived as follows: treating the circuit as a voltage divider, the output network consisting of capacitor and R_L has an impedance of:

$$Z_2 = (1/sC + R_C) \,||\, R_L = \frac{(1/sC + R_C)\cdot R_L}{(1/sc + R_C) + R_L} = R_L \cdot \frac{sR_C C + 1}{s(R_C + R_L)C + 1}$$

The impedance of the input network, L, is $Z_1 = sL$. Then the transfer function is the divider ratio:

$$\frac{v_o}{v_i} = \frac{Z_2}{Z_1 + Z_2} = \frac{sR_C C + 1}{s^2 LC\left(\frac{R_C}{R_L} + 1\right) + s\left(\frac{L}{R_L} + R_C C\right) + 1}$$

This response has a zero at $1/R_C{\cdot}C$ and a pole-pair with pole frequency:

$$\omega_n = \frac{1}{\sqrt{LC\left(\frac{R_C}{R_L}+1\right)}}$$

and a damping ratio of:

$$\zeta = \frac{1}{2\cdot Q} = \frac{1}{2}\cdot\left(\sqrt{\frac{L/C}{R_L\cdot(R_C+R_L)}}+\sqrt{\frac{R_C\cdot(R_C+R_L)}{L/C}}\right)$$

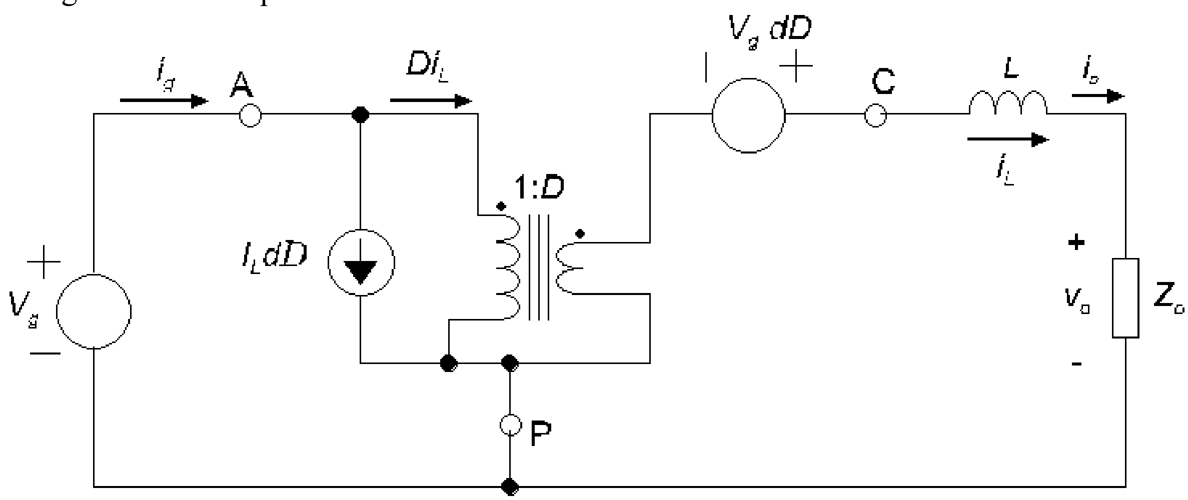
where, the pole angle is $\phi = \cos^{-1}\zeta$.

The pole angle is minimum (and damping, ζ, is maximum) when:

$$Z_n = \sqrt{\frac{L}{C}} = (R_C+R_L)\cdot\sqrt{R_C\cdot R_L}$$

Incremental Converter Model: Voltage Control

The following circuit is the quintessential buck converter with the incremental switch model.



For voltage control, the independent (controlling) variable is duty ratio and the controlled variable is the output voltage. With a generalized output load impedance, Z_o, the transfer function is derived from the following circuit equations:

$$v_o = i_L \cdot Z_o$$
$$v_L = sL\cdot i_L = V_g\cdot dD - v_o \Rightarrow v_o = V_g\cdot dD - sL\cdot i_L$$
$$i_g = I_L\cdot dD + D\cdot i_L$$

Equate v_o:

$$i_L\cdot Z_o = V_g\cdot dD - sL\cdot i_L$$

Then solving for the first transfer function:

$$\frac{i_L}{dD} = \frac{i_o}{dD} = \frac{V_g}{sL+Z_o}$$

Furthermore:

$$\frac{v_o}{dD} = \frac{v_o}{i_L} \cdot \frac{i_L}{dD} = Z_o \cdot \frac{i_L}{dD}$$

Substituting:

$$\frac{v_o}{dD} = \frac{Z_o}{sL + Z_o} \cdot V_g$$

The third needed transfer function is:

$$\frac{i_g}{dD} = I_L + D \cdot \frac{i_L}{dD}$$

or:

$$\frac{i_g}{dD} = \frac{V_o}{R_o} + \frac{V_o}{sL + Z_o} = \frac{V_o}{R_o \parallel (sL + Z_o)}, R_o = \mathrm{Re}\{Z_o\}$$

The output impedance is modeled as a load resistance, R_L, shunting the filter capacitor. It is modeled as a capacitance, C, in series with internal capacitor resistance, R_C. Then:

$$Z_o = R_L \cdot \frac{sR_C C + 1}{s(R_C + R_L)C + 1}$$

and:

$$\frac{i_o}{dD} = \frac{V_g \cdot (s \cdot [R_C + R_L] \cdot C + 1)}{sL \cdot (s \cdot [R_C + R_L] \cdot C + 1) + R_L \cdot (sR_C C + 1)} = \frac{V_g}{R_L} \cdot \frac{s(R_C + R_L) \cdot C + 1}{s^2 LC \cdot \left(\frac{R_C + R_L}{R_L}\right) + sR_C C + 1}$$

Substituting again for Z_o:

$$\frac{v_o}{dD} = V_g \cdot \frac{sR_C C + 1}{s^2 LC \cdot \left(\frac{R_C + R_L}{R_L}\right) + sR_C C + 1}$$

and:

$$\frac{i_g}{dD} = \frac{V_o}{R_o} + \frac{V_o}{R_L} \cdot \frac{s(R_C + R_L) \cdot C + 1}{s^2 LC \cdot \left(\frac{R_C + R_L}{R_L}\right) + sR_C C + 1}$$

The transfer function from input to output for the current can be derived from two previous transfer functions. After some algebra:

$$\frac{i_o}{i_g} = \frac{V_g}{V_o} \cdot \frac{R_o}{R_o + R_L} \cdot \frac{s(R_C + R_L) \cdot C + 1}{s^2 LC \cdot \left(\frac{R_C + R_L}{R_o + R_L}\right) + s(R_C + R_o \parallel R_L) \cdot C + 1}$$

One other transfer function that will be of interest is derived from:

$$D \cdot v_g + V_g \cdot dD = v_o + sL \cdot \left(\frac{v_o}{Z_o}\right) = v_o + sL \cdot i_o$$

Then:

$$\frac{v_o}{v_g} = D \cdot \frac{Z_o}{sL + Z_o}, dD = 0$$

These are the relevant transfer functions that can now be used in the incremental circuit model. The pole characterization can be expressed as:

$$\zeta = \frac{1}{2} \cdot \frac{\sqrt{R_C \cdot (R_C \parallel R_L)}}{Z_n} \cong \frac{1}{2} \cdot \frac{R_C}{Z_n}, R_C << R_L$$

where:

$$Z_n = \sqrt{\frac{L}{C}}$$

The pole angle is then $\phi = \cos^{-1} \zeta$ and the pole magnitude is:

$$\omega_n = \frac{1}{\sqrt{L \cdot C}}$$

With all blocks of the diagram determined, feedback analysis can be performed. The loop gain is the product of the transfer functions around the loop. Its poles and zeros determine stability. Additional zeros and poles and static (dc) loop gain needed in $A_c(s)$ are determined by using Bode or root-locus plots and applying control theory to circuits. The above circuit diagram does not include $A_c(s)$, as drawn. An op-amp stage for $A_c(s)$ would include the error summing function and the stage would output v_e as input to the PWM circuit.