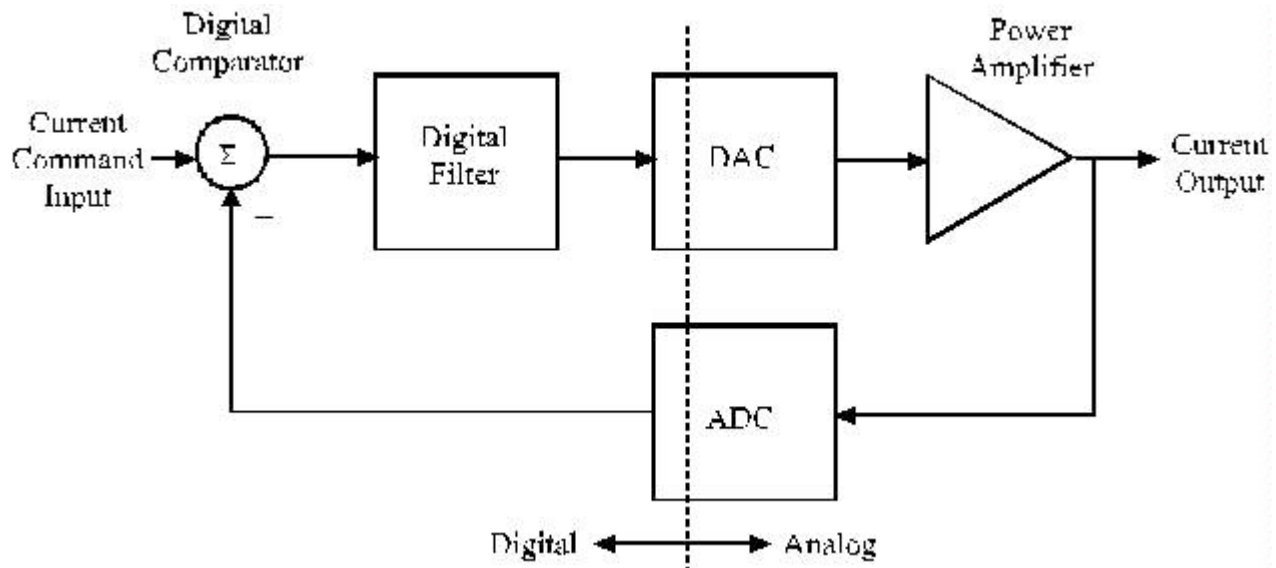


Design Techniques for New Engineers
How to Regard ADCs and DACs in Circuits
by Dennis L Feucht

One of the confusing aspects of circuit design involves circuits with multiple representations of variable values. Circuits commonly have both analog and digital components and with analog-to-digital (A/D) converters (ADCs) and D/A converters (DACs), voltages and currents that are functions of time (or *waveforms*) appear in both analog (continuous) and digital (discrete) representations.

To appreciate the problems that can arise, consider a simple example of an analog and digital (or *mixed-signal*) system as shown below.



In this system, an analog output device (which could be a motor or a loudspeaker) is within a feedback loop. In the feedback path, an ADC converts the output current to a digital value of n bits. This quantity representing the current is then compared to the commanded value, also digital, and the error processed by a digital filter. Its output is D/A converted to an analog waveform which drives the power amplifier. The digital filter performs digital amplification, with various poles and zeros in its frequency response, to compensate the dynamic response of the loop. Its output is then converted to an analog voltage which drives a power transconductance (voltage in, current out) amplifier. How can we analyze this feedback loop with digital processing in it?

The ADC

Let's start by analyzing one component, the ADC. In this case, it has n digital output bit-lines, plus transfer lines, and one analog input voltage. One way of considering ADCs is that their digital output ratio equals their analog input ratio:

$$\frac{w_o}{2^n} = \frac{v_i}{V_R}$$

where, n is the number of bits of the ADC, and 2^n is the digital range of w_o , the output digital value. This fraction is the same as the (analog) input voltage, v_i , over the reference voltage, V_R . The value of w_o is:

$$w_o = \left(\frac{2^n}{V_R} \right) \cdot v_i$$

This value has no units, though it represents v_i . Or does it? It represents the fraction that v_i is of V_R . In using an ADC, we want to acquire v_i in digital form. Yet what we actually have is a unitless fraction.

The ADC digital output, w_o , is not the desired digital voltage value but is a fraction of 2^n , part of a digital ratio. On the digital side of the ADC, we must "undo" the scaling that occurred in the ADC to recover the value of v_i . If in the μC we perform the inverse ADC function on w_o the result should be a digital voltage of value equal to v_i :

$$v_i = \left(\frac{V_R}{2^n} \right) \cdot w_o$$

This inverse function is an additional block following the ADC, though not shown above, and might be labeled "ADC⁻¹". Looked at from this equation, the ADC is simply an amplifier with a static (dc) gain equal to the scale ratio. By representing V_R as 2^n , then each LSB of digital value is equal to $V_R \cdot 2^{-n}$. The recovered digital value of the analog input voltage is $(V_R \cdot 2^{-n}) \cdot w_o$.

Now let the ADC input voltage have a range of -5 V at negative full-scale ($-fs$) and $+5\text{ V}$ at $+fs$ with 0 V at zero-scale (zs). On the digital side, digital numbers are usually represented in two's complement arithmetic, though the interpretation of the digital values depends on the corresponding analog values. If the ADC block above includes in it not only the ADC core but also an op amp circuit that offsets the analog value for a bipolar range, then the transfer function is affected by this mid-scale offset and this affects the interpretation of the digital input value.

Consider that the transfer function for the three points in its range are given in the table below, with some possible digital values.

Analog Input, V	Two's Complement Output	Offset Binary Output
-5 V ($-fs$)	-2048 (800 hex)	0
0 V (zs)	0	2048 (800 hex)
$+5\text{ V}$ ($+fs$)	2047 (7FF hex)	4095 (FFF hex)

Then the transfer function of the ADC -- at least the static factor of it -- becomes $(V_R/2^{n-1})$ and the range is $\pm(V_R/2^{n-1})$.

ADC Transfer Function

The static transfer function of the ADC is also its quasistatic (low-frequency ac) gain. Furthermore, ADCs have a dynamic gain factor involving s -domain poles. This is caused by the sampling nature of ADCs. Dynamically, they are sample-and-hold devices. The sample-and-hold electronics cannot be separated physically, but conceptually it is appealing to separate them into two cascaded functional blocks.

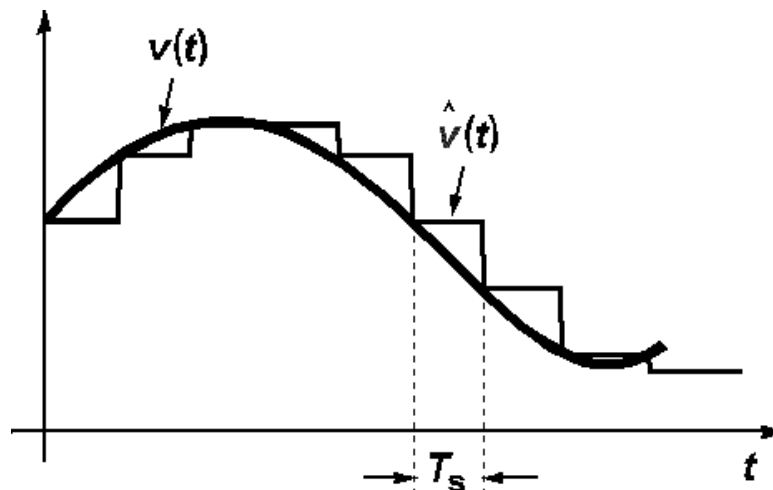
The sampler converts a voltage or current waveform, $x(s)$, into $x^*(s)$, a sequence of impulses spaced apart in time by T_s . A time delay of $k \cdot T_s$ of waveform $x(t)$, or $x(t - k \cdot T_s)$, is Laplace-transformed to $x(s) \cdot \exp(-s \cdot (k \cdot T_s))$:

$$x^*(s) = \sum_{k=0}^{\infty} x(k \cdot T_s) \cdot e^{-s \cdot (k \cdot T_s)}$$

The sampler is followed conceptually by a hold function, $H_0(s)$:

$$H_0(s) = \frac{1 - e^{-s \cdot T_s}}{s \cdot T_s}$$

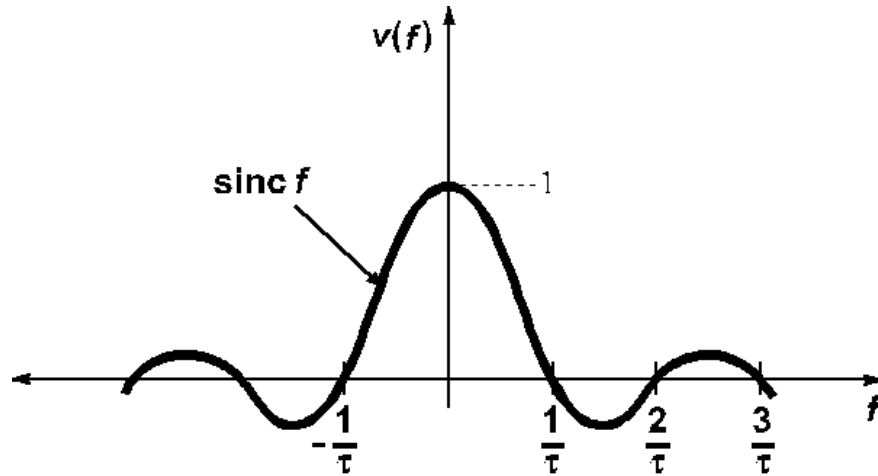
This is the gain-normalized integration ($1/s \cdot T_s$) of an impulse train in the time domain, resulting in a step function turned off T_s later. At each sample time, a new value of ADC output is acquired and held in the μC . Plotted against time, this waveform has the stair-step look of a sample-and-hold waveform, described by $H_0(s)$. The acquired voltage waveform, $v(t)$, is shown below, plotted along with the $\hat{v}(t)$ “stair-step” acquisition. If an approximation of the acquired waveform is reconstructed by shifting the continuous waveform by $T_s/2$ to the right, it passes through the centers of the vertical steps of the acquired ZOH waveform.



Discrete-time samples at sample rate $f_s = 1/T_s$ have a frequency response of:

$$\frac{\sin(\omega \cdot T_s / 2)}{\omega \cdot T_s / 2} = \frac{\sin(\pi \cdot \frac{f}{f_s})}{\pi \cdot \frac{f}{f_s}}$$

This function is shown below.



This response can be compensated with an inverse ZOH (ZOH^{-1}) function (not shown, but possibly included following the ZOH block). It can be omitted if the ADC sample rate is sufficiently greater than the loop bandwidth to make amplitude roll-off and phase delay insignificant.

The ADC sample-and-hold frequency response is the magnitude and phase of $H_0(j\omega)$:

$$H_0(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega \cdot T_s} = \frac{\sin(\omega \cdot T_s / 2)}{\omega \cdot T_s / 2} \cdot e^{-j\omega T_s / 2} = \frac{\sin(\pi \cdot f / f_s)}{\pi \cdot f / f_s} \cdot e^{-j\pi \cdot f / f_s}$$

where the amplitude is:

$$|H_0(j\omega)| = \left| \frac{\sin(\omega \cdot T_s / 2)}{\omega \cdot T_s / 2} \right| = \left| \frac{\sin(\pi \cdot f / f_s)}{\pi \cdot f / f_s} \right|$$

and the phase is:

$$\angle H_0(j\omega) = -\frac{\omega \cdot T_s}{2} + \theta = -\pi \cdot f / f_s + \theta, \quad \theta = \begin{cases} 0, & \sin(\omega \cdot T_s / 2) > 0 \\ \pi, & \sin(\omega \cdot T_s / 2) < 0 \end{cases}$$

More simply, the phase is $-180^\circ \cdot (f/f_s)$, where $f_s = 1/T_s$.

At the Nyquist frequency, $f_s/2$, the magnitude will have decreased to $(\sin(\pi/2))/(\pi/2) = 2/\pi \approx 0.636$ with a phase delay of $180^\circ/10 = 18^\circ$. A sampling rate of 10 times f_s results in a normalized amplitude of 0.9836, or about 6 bits in accuracy. Some values are given in the following table.

f/f_s	$\omega \cdot T_s / 2 = \pi \cdot (f/f_s)$	$\sin(\omega \cdot T_s / 2) / (\omega \cdot T_s / 2)$	$\angle H_0(j\omega), ^\circ$
1.00	$\pi/1$	0	-180
0.50	$\pi/2$	0.636	-90
0.33	$\pi/3$	0.827	-60
0.25	$\pi/4$	0.900	-45
0.20	$\pi/5$	0.936	-36
0.167	$\pi/6$	0.955	-30
0.125	$\pi/8$	0.975	-22.5
0.10	$\pi/10$	0.984	-18

In a control loop, the ADC dynamic response can have a significant effect upon loop behavior, depending on f/f_s . DACs have the same transfer function characteristics as ADCs: a quasistatic gain of the same form, except that the analog ratio is the output, and the $\sin\theta/\theta$ dynamic behavior. For the DAC, this can be compensated digitally by a software function of ZOH^{-1} preceding the DAC if the f/f_s value is known.

