

MOSFET Voltage Optimization

by Dennis L Feucht

Q: Is there an optimum MOSFET voltage for power electronics applications that will minimize power loss?

A: This question falls in the general category of impedance matching in that an optimal voltage-current tradeoff point, or impedance, is sought. This arises not only in the more common circuit applications where the maximum-power-transfer theorem is applied (such as calculation of a transformer turns ratio), but also in less obvious applications such as the driver output impedance driving a motor to match the mechanical impedance as referred to the electrical side of the machine.

For MOSFET voltage optimization, we need to formulate a more rigorous definition of the problem. Power loss can be minimized by not powering the MOSFET, but that is the uninteresting degenerate solution. What we're really after is minimization of a figure of demerit that can be defined as the ratio:

$$\frac{\text{power loss}}{\text{power switched}} = \frac{r_{on} \cdot i_D^2}{v_{DS} \cdot i_D} = \frac{r_{on} \cdot i_D}{v_{DS}}$$

This is simply the voltage ratio of off- to on-voltage across the MOSFET. It is minimized by minimizing i_D and maximizing the rated v_{DS} .

The on resistance, r_{on} , of MOSFETs, as Motorola (now ON Semiconductor) has published in the past in MOSFET data books is:

$$r_{on} \propto V_{DS}^{2.5}$$

MOSFET on-resistance increases superlinearly with drain-source voltage. The figure of demerit thus becomes:

$$\frac{\text{power loss}}{\text{power switched}} = \frac{r_{on} \cdot i_D}{v_{DS}} \propto i_D \cdot v_{DS}^{1.5}$$

On-resistance also varies superlinearly with current, and increasingly so for higher-voltage MOSFETs. The figure of demerit as given above assumes that it varies linearly with i_D -- that its exponent is one. But what is it really?

In good design, generally the MOSFET current and voltage ratings are fully used in that the MOSFET has no additional, unused power-switching capability. This is the optimal use of any power part, with some reliability margin included in the choice of maximum switching power.

To illustrate this from MOSFET data (taken from the Motorola TMOS data book, DL135/D REV6), consider TO-220-packaged n-channel MOSFETs. A MTP3N100E is rated at 1 kV, 3 A with $r_{on} = 4.0 \Omega$ at 1.5 A and 125 W maximum power dissipation. A similarly power-rated MOSFET at 125 W is the MTP27N10E, rated at 100 V, 27 A with $r_{on} = 70 \text{ m}\Omega$ at 13.5 A. The ratios for each are:

$$\text{MTP3N100E} \frac{\text{power loss}}{\text{power switched}} = \frac{(4.0 \Omega) \cdot (1.5 \text{ A})^2}{(1 \text{ kV}) \cdot (1.5 \text{ A})} = \frac{9 \text{ W}}{1500 \text{ W}} = 6 \times 10^{-3}$$

$$\text{MTP27N10E} \frac{\text{power loss}}{\text{power switched}} = \frac{(70 \text{ m}\Omega) \cdot (13.5 \text{ A})^2}{(100 \text{ V}) \cdot (13.5 \text{ A})} = \frac{12.76 \text{ W}}{1350 \text{ W}} = 9.5 \times 10^{-3}$$

Comparing these MOSFETs, it would appear that MOSFETs are more efficient as high-resistance (high voltage, low current) devices. This is not what the figure of demerit would suggest if it varies linearly with i_D , as given above. As shown by the above two MOSFETs, the exponent of i_D must be larger than that of v_{DS} for the high-R MOSFET to have the lower figure of demerit.

Therefore, the notion that MOSFETs are better as low-R devices is not always true. In practice they often are because IGBTs have an additional junction voltage drop that offsets them toward higher voltages for more efficiency, usually over 200 V. BJTs, such as Darlingtons, have the complication of saturating the output transistor without returning the collector of the driving transistor to a higher voltage. BJTs have a higher current density than MOSFETs and should be optimal for low-R applications. However, the additional complication of the base-drive current makes MOSFETs generally easier to apply.

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