

## **The Future of Electrical Signaling in a Post-10 Gbit/s World**

*Defining and overcoming the challenges of high-speed serial interfaces for networking and interconnect applications*

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For the past ten years electrical signaling has been progressing at a furious pace. Wide single-ended interfaces were replaced with narrower, faster, interfaces based on high speed differential signals. For example, the IEEE 802.3 10 Gigabit Ethernet specification introduced the XAUI (10 Gigabit Attachment Unit Interface), a full duplex interface based on four differential pair operating at 3.125 Gbit/s each that provides 10 Gbit/s throughput in each direction. With its compact interface and extended reach capabilities, the XAUI quickly found its way into chip-to-chip, chip-to-module, and backplane applications.

With the introduction of XAUI system providers sought to increase the capabilities of backplanes in the field, therefore pushing out the need for customers to do forklift upgrades. Many of these systems proved incapable, and system providers found themselves faced with developing new backplanes and systems. This sparked off research and development efforts into all aspects of component technology and system development.

The exponential requirements of bandwidth soon forced the need for something beyond XAUI. The High Speed Backplane Initiative was the first body to recognize the need for something beyond XAUI and targeted 6.25 Gbit/s serial speeds for backplanes. This effort was absorbed into and became part of the Optical Networking Forum's Common Electrical I/O project, which targeted 6+ and 11+ Gbit/s. Ultimately, completing the circle, was the IEEE 802.3ap Backplane Ethernet project, which standardized operation across a backplane environment in support of Gigabit and 10 Gigabit Ethernet MAC rates, and provided a serial 10 Gbit/s PHY, known as 10GBASE-KR.

Having been personally involved with the efforts described in the paragraph above I know those words do not give adequate justice to the time, money, and effort given by so many individuals from so many various companies and industries. I can say that I am proud to have been part of that industry effort, which is ultimately having a positive impact on the world. Given the opportunity in this column, I would like to take a moment to thank all my colleagues for their time, patience, efforts, and support over the years, as we pursued making reliable 10G serial transmission a reality.

With that said, discussion of rates beyond 10 Gbit/s is beginning to show up. Discussion regarding the future of FibreChannel targets 17 Gbit/s rates, while the Optical Internetworking Forum has the CEI-25 project that is targeting 20 to 25 Gbit/s rates for chip-to-chip and backplane applications. And it is not difficult to envision an interface for 100 Gbit/s Ethernet that is similar to XAUI, based on 4 lanes of 25 Gbit/s. But as we move forward, the development efforts of the past hold insight for the future.

During the development of 10GBASE-KR it was found that it is the combined interactive performance between the active and passive aspects of the system interconnect that will determine whether a serial rate can be achieved. As designs approach and go beyond serial 10 Gbit/s rates, the strength of any single aspect of the system interconnect will not make it work. On the contrary -- the weakness of any single aspect of the system interconnect will make it not work. Therefore, development efforts underway related to the passive and active aspects of the system interconnect must be considered. The active and passive aspects of the system

interconnect are interdependent, and are interlinked with the modeling, design, and characterization of the system interconnect.

The system interconnect varies by application and is driven by the economics and constraints of the application. Therefore, from the passive aspect, the connectors, cable assemblies, PCB materials, and PCB fabrication techniques should be considered on an application-by-application basis. The active aspect of the system interconnect, which also varies by application space, is the signaling solution; ie the signaling scheme and equalization techniques used at the transmitter and receiver. The design of the system interconnect will vary according to the application, but understanding the limitations of the system interconnect can aid in the development of a system that has an architecture with a higher chance of success. Ironically, it is the characterization of the system interconnect that is fairly consistent with application.

The development of signaling beyond 10 Gbit/s will require perspectives from a range of diverse backgrounds. The focus of this series will be to start asking questions, and not to provide answers. By understanding the future development paths of the passive and active aspects of the system interconnect, we will be able to understand the hurdle that the passive structure will provide and the capabilities of the active aspect of the system interconnect in overcoming that hurdle.

To provide insight into the future of these different areas, a group of distinguished colleagues will provide a series of articles over the coming months:

- Adam Healey, Consulting Member of Technical for LSI, will leverage off his experience as the former chair of the IEEE 802.3ap Backplane Ethernet, and provide his perspective on the lessons learned for the development of a signaling specification
- Gourgen Oganessyan, Senior Signal Integrity Engineer at Molex, will discuss where connectors are going for backplane applications
- Mike Fogg, Senior Member of Technical Staff at Tyco Electronics, will share his thoughts on creating cable assemblies for 25 Gbit/s data rates
- Silvio Bertling, a Technologist at Park Nelco, will explore the future of properties for PWB materials
- Joel Goergen, Vice President of Technology and Chief Scientist from Force10 Networks, will provide insight into system architectures and how they take the system interconnection into consideration
- Mike Resso, a Signal Integrity Expert in the Signal Integrity Applications Group at Agilent Technologies, and Sanjeev Gupta, a Signal Integrity Expert at EEsosof, will discuss the role of testing, characterization, and modeling of the passive interconnect
- David Stauffer, IBM Senior Technical Staff Member and the Optical Internetworking Forum Physical and Link Layer Working Group Chair, will close things out by looking at the active portion of the problem, and discuss what lies ahead for 25 Gbit/s signaling.

Together we are taking the first steps on a journey towards the future, a journey which starts with questions. It is also a journey where we must take the steps together, because the solution will lie in the integration of the parts of the system interconnect, its design, and its characterization. Since you have taken the time to read this, you are part of the journey, and are encouraged to participate, and to ask questions.

Feel free to comment on the series with your suggestions or questions by contacting John D'Ambrosia at [jdambrosia@ieee.org](mailto:jdambrosia@ieee.org)

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